



Product Qualification Report

Product Qualification Report

STK17T88 Revision B

Issue 00 Dated 10 August 2006

Ref PCN10062 Device Revision & Datasheet Change

SUMMARY

The design and process for this product were modified to resolve number of issues found in the initial product release. Simtek PCN 10062, attached, outlines these changes. The qualification data for the new revision is in Table I. The datasheet characterization data is in Table II.

PRODUCT AFFECTED

STK17T88 RTC with 256K nvSRAM.

All package types.

Commercial and Industrial grades.

NEW PRODUCT DESIGN REV ID

Product built using the new design and process revisions will be marked "Simtek B" on the first line of the topside mark.

PCN REFERENCES Posted on Simtek website at www.simtek.com

Simtek PCN10062, Datasheet Changes STK17T88 3V Event Data Recorder. Copy attached to this report.

New datasheet: ML0024 Revision 1.6.

PRODUCT CHANGES

A number of changes to design and process were implemented in this version of the product in order to optimize non-volatile functionality. Lifetest data from the re-design qualification is provided in Table II of this report. A number of changes to datasheet have been made as documented in the above-referenced PCN. These are also itemized in the change history section of the revised datasheet as referenced above.



Qualification Status Report

Table I Qualification Lifetest Report

[Lifetest samples from 3 separate wafer fab lots]

Stress	Method	# of Lots	SS/Lot	C=	Conditions	Duration	Result
High Temp Operating Life	JA108	3	77	0	140C External Vcc 3.6V Internal regulated 2.4V	352hr	231/0
Store Cycle Endurance [1]	STK	1	63	0	Software induced store operations	200K cycles	63/0
Store Cycle Endurance [2]	STK	1	64	0	Autostore [power cycle] induced store operations	200K cycles	64/0
High Temp Retention Bake	JA103	1	77	0	200C unbiased bake, store data in nv array. Recall data after bake.	20years @ 55C	77/0
Electrostatic Discharge HBM	M3015	1	9	0	1750V		Pass
Electrostatic Discharge CDM	JC101	1	6	0	500V		Pass
Latch-Up	JESD78	1	6	0	+/- 200mA, 85C		Pass
I/O Capacitance & Guaranteed DS Parameters	STK	1	6	0	To datasheet		Pass
Datasheet Characterization	STK	3	15	Cpk>1.33	-40C to +85C		Pass
Physical Dimensions [each pkg]	M2016	1	15	Cpk>1.66	Per package outlines		Pass
Preconditioning	JA113	Per MSL level tested.			Per J-STD-020 and JEDEC22-A113		
MSL Classification	J-STD-020	3	11	0	Per J-STD-020 for lead-free 260C peak reflow		MSL3 @ 260C
Temperature Cycling [pc]	JA104	3	45	0	-65C to +150C, 10min dwell	500 cyc	MSL3 @ 260C
Autoclave/PCT [pc]	JA102	3	45	0	121C/100%RH/2atm	96hr	MSL3 @ 260C
Material Analysis	RoHS				Materials meet RoHS requirements. ICP reports on file.		
Datasheet Changes					ML0024 Rev 1.6		
Change Notification					PCN10062		

			SPEC		-40C		0C		25C		70C		85C		Margin to Spec (-I)	Margin to Spec (-C)	Notes
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
READ CYCLE																	
ELQV	1	Chip Enable Access Time		45ns	24.2ns	30.6ns	26.0ns	32.4ns	27.0ns	33.4ns	32.4ns	34.4ns	30.4ns	37.4ns	7.6ns	10.6ns	
AVAVR	2	Read Cycle Time	45ns		21.0ns	26.6ns	23.0ns	28.4ns	24.2ns	29.6ns	29.4ns	30.8ns	27.6ns	33.8ns	11.2ns	14.2ns	
AVQV	3	Address Access Time		45ns	25.0ns	29.8ns	26.6ns	32.2ns	27.6ns	33.4ns	33.2ns	34.6ns	31.4ns	37.6ns	7.4ns	10.4ns	
GLOV	4	Output Enable to Data Valid		20ns	5.6ns	8.4ns	5.8ns	8.8ns	6.0ns	9.0ns	7.2ns	9.2ns	6.8ns	10.0ns	10.0ns	10.8ns	
AXQX	5	Output Hold after Address Change	3ns		7.4ns	10.0ns	7.8ns	10.4ns	8.0ns	10.6ns	9.2ns	10.8ns	8.6ns	11.4ns	4.4ns	4.8ns	
ELQX	6	Chip Enable to Output Active	3ns		25.4ns	32.6ns	27.0ns	36.0ns	28.2ns	37.8ns	33.2ns	40.0ns	31.4ns	42.8ns	22.4ns	24.0ns	
EHQZ	7	Chip Enable to Output Inactive		15ns	6.4ns	7.8ns	6.8ns	8.4ns	6.8ns	8.8ns	8.2ns	9.0ns	7.6ns	9.4ns	5.6ns	6.0ns	
GLOX	8	Output Enable to Output Active	0ns		6.2ns	10.6ns	6.8ns	11.8ns	6.8ns	12.6ns	7.8ns	14.4ns	7.4ns	15.0ns	6.2ns	6.8ns	
GHQZ	9	Output Enable to Output Inactive		15ns	6.4ns	7.6ns	6.6ns	8.2ns	6.8ns	8.6ns	8.0ns	8.8ns	7.4ns	9.4ns	5.6ns	6.2ns	
ELICCH	10	Chip Enable to Power Active	0ns														
EHICCL	11	ChipDisable to Power Standby		45ns													
WRITE CYCLE #1 (W/ Controlled)																	
AVAV	12	Write Cycle Time	45ns														
WLWH	13	Write Pulse Width	30ns		6.2ns	8.0ns	6.6ns	8.2ns	6.6ns	8.4ns	7.4ns	8.2ns	7.0ns	9.0ns	21.0ns	21.6ns	
ELWH	14	Chip Enable to End of Write	30ns		5.2ns	7.2ns	5.4ns	7.6ns	5.6ns	7.6ns	6.4ns	7.6ns	6.2ns	8.2ns	21.8ns	22.4ns	
DVWH	15	Data Set-up to End of Write	15ns		5.2ns	6.8ns	5.4ns	7.4ns	5.8ns	7.4ns	6.8ns	7.6ns	6.4ns	8.4ns	6.6ns	7.4ns	
WHDX	16	Data Hold after End of Write	0ns		-3.0ns	-2.2ns	-3.2ns	-2.2ns	-3.2ns	-2.4ns	-3.2ns	-3.2ns	-4.0ns	-2.8ns	2.2ns	2.2ns	
AVWH	17	Address Set-up to End of Write	30ns		4.4ns	6.8ns	4.6ns	7.0ns	4.6ns	7.2ns	5.2ns	5.2ns	5.0ns	6.2ns	22.8ns	22.8ns	
AVWL	18	Address Set-up to Start of Write	0ns		-3.2ns	-2.4ns	-3.4ns	-2.6ns	-3.6ns	-2.8ns	-3.8ns	-3.6ns	-4.2ns	-3.4ns	2.4ns	2.6ns	
WHAX	19	Address Hold after End of Write	0ns		-2.2ns	-1.8ns	-2.4ns	-1.8ns	-2.2ns	-2.0ns	-2.2ns	-2.2ns	-2.4ns	-2.2ns	1.8ns	1.8ns	
WLQZ	20	Write Enable to Output Disable		15ns	6.8ns	9.0ns	7.2ns	9.6ns	7.2ns	10.0ns	8.4ns	10.2ns	8.0ns	11.0ns	4.0ns	4.8ns	
WHQX	21	Output Active after End of Write	3ns		26.8ns	41.4ns	29.2ns	41.6ns	30.4ns	41.4ns	35.8ns	41.2ns	34.2ns	43.4ns	23.8ns	26.2ns	
WRITE CYCLE #2 (E/ Controlled)																	
AVAV	12	Write Cycle Time	45ns														
WLEH	13	Write Pulse Width	30ns		4.4ns	6.2ns	4.6ns	6.4ns	4.8ns	6.6ns	5.4ns	6.2ns	5.0ns	7.2ns	22.8ns	23.4ns	
ELEH	14	Chip Enable to End of Write	30ns		6.0ns	7.8ns	6.2ns	8.0ns	6.6ns	8.0ns	7.2ns	8.0ns	6.8ns	8.8ns	21.2ns	22.0ns	
DVEH	15	Data Set-up to End of Write	15ns		4.8ns	6.6ns	5.2ns	6.8ns	5.2ns	6.8ns	6.6ns	7.2ns	6.0ns	7.8ns	7.2ns	7.8ns	
EHDH	16	Data Hold after End of Write	0ns		-2.4ns	-1.8ns	-2.6ns	-2.0ns	-2.8ns	-2.2ns	-2.8ns	-2.6ns	-3.2ns	-2.2ns	1.8ns	2.0ns	
AVEH	17	Address Set-up to End of Write	30ns		4.0ns	6.8ns	4.4ns	7.0ns	4.4ns	7.2ns	4.8ns	4.8ns	4.6ns	6.0ns	22.8ns	22.8ns	
AVEL	18	Address Set-up to Start of Write	0ns		-3.2ns	-2.4ns	-3.6ns	-2.8ns	-3.8ns	-3.0ns	-3.8ns	-3.8ns	-4.4ns	-3.4ns	2.4ns	2.8ns	
EHAX	19	Address Hold after End of Write	0ns		-2.0ns	-1.4ns	-2.0ns	-1.6ns	-2.2ns	-1.6ns	-2.0ns	-2.0ns	-2.2ns	-1.8ns	1.4ns	1.6ns	
NV PARAMETERS																	
AVAV	26	CE Controlled Initiation Cycle Time (Soft Seq)	45ns														
AVAV	26	OE Controlled Initiation Cycle Time (Soft Seq)	45ns														
AVELN	27	Address Set-up to Start of Write (Soft Seq)	0ns														
AVGL	27	Address Set-up to Start of OE (Soft Seq)	0ns														
ELEHN	28	Chip Enable to End of Write (Soft Seq)	30ns														
GLGH	28	Output Enable Pulse Width (Soft Seq)	30ns														
ELAX	29	Address Hold after CE low (Soft Seq)	0ns														
GLAX	29	Address Hold after OE low (Soft Seq)	0ns														
ELQXS	23	Store Cycle Duration (Soft Seq)		15ms													
ELQXR	30	Recall Cycle Duration (Soft Seq)		50us													
VCCRISE	25	VCC Rise Time	150us														
DELAY	31	Time to Complete SRAM Cycle	1us														
HLHH	32	Hardware Store Pulse Width	15ns														
HLBL	33	Hardware Store Low to Store Busy		300ns													
DC CHARACTERISTICS																	
ICC1		Average Vcc Current @ AVAV=45ns		50mA	29.2mA	41.3mA	29.4mA	39.5mA	29.4mA	38.5mA	29.7mA	35.4mA	29.3mA	36.1mA	8.7mA	10.5mA	
ICC2		Average Vcc Current During Store		3mA	1.1mA	1.6mA	1.4mA	1.8mA	1.5mA	1.9mA	2.0mA	2.1mA	1.9mA	2.4mA	0.6mA	0.9mA	
ICC3		Average Vcc Current @200ns		10mA													
ICC4		Average Vcc Current during Autostore		3mA													
ISB		Vcc Standby Current		3mA	1.1mA	1.7mA	1.2mA	1.8mA	1.3mA	1.8mA			1.3mA	2.0mA	1.0mA	1.2mA	
ILKG		Input Leakage Current	-1uA	1uA													
IOLKG		Off-State Output Leakage Current	-1uA	1uA													
VIH		Input Logic "1" Level	2.0V														
VIL		Input Logic "0" Level		0.8V													
VOH		Output Logic "1" Voltage	2.4V		2.6V	3.5V	2.5V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	0.1V	0.1V	
VOL		Output Logic "0" Voltage		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.2V	0.2V	0.3V	
VOLBU		Logic "0" Voltage on HSB1 Output		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VSWITCH	24	Autostore Trigger Point		2.65V	2.49V	2.56V	2.51V	2.60V	2.52V	2.58V			2.56V	2.61V	0.04V	0.05V	

No Data