



Product Qualification Report

Product Qualification Report

STK17TA8 Revision B

Issue 00 Dated 10 August 2006

Ref PCN10061 Device Revision & Datasheet Change

SUMMARY

The design and process for this product were modified to resolve number of issues found in the initial product release. Simtek PCN 10062, attached, outlines these changes. The qualification data for the new revision is in Table I. The datasheet characterization data is in Table II.

PRODUCT AFFECTED

STK17TA8 RTC with 1M nvSRAM.

All package types.

Commercial and Industrial grades.

NEW PRODUCT DESIGN REV ID

Product built using the new design and process revisions will be marked "Simtek B" on the first line of the topside mark.

PCN REFERENCES Posted on Simtek website at www.simtek.com

Simtek PCN10061, Datasheet Changes STK17TA8 3V Event Data Recorder. Copy attached to this report.

New datasheet: ML0025 Revision 1.4.

PRODUCT CHANGES

A number of changes to design and process were implemented in this version of the product in order to optimize non-volatile functionality. Lifetest data from the re-design qualification is provided in Table II of this report. A number of changes to datasheet have been made as documented in the above-referenced PCN. These are also itemized in the change history section of the revised datasheet as referenced above.



Qualification Status Report

Table I Qualification Lifestest Report

[Lifestest samples from 3 separate wafer fab lots]

Stress	Method	# of Lots	SS/Lot	C=	Conditions	Duration	Result
High Temp Operating Life	JA108	3	77	0	140C External Vcc 3.6V Internal regulated 2.4V	352hr	230/0
Store Cycle Endurance [1]	STK	1	64	0	Software induced store operations	200K cycles	64/0
Store Cycle Endurance [2]	STK	1	64	0	Autostore [power cycle] induced store operations	200K cycles	64/0
High Temp Retention Bake	JA103	1	77	0	200C unbiased bake, store data in nv array. Recall data after bake.	20years @ 55C	77/0
Electrostatic Discharge HBM	M3015	1	9	0	1750V		Pass
Electrostatic Discharge CDM	JC101	1	6	0	500V		Pass
Latch-Up	JESD78	1	6	0	+/- 200mA, 85C		Pass
I/O Capacitance & Guaranteed DS Parameters	STK	1	6	0	To datasheet		Pass
Datasheet Characterization	STK	3	15	Cpk>1.33	-40C to +85C		Pass
Physical Dimensions [each pkg]	M2016	1	15	Cpk>1.66	Per package outlines		Pass
Preconditioning	JA113	Per MSL level tested.			Per J-STD-020 and JEDEC22-A113		
MSL Classification	J-STD-020	3	11	0	Per J-STD-020 for lead-free 260C peak reflow		MSL3 @ 260C
Temperature Cycling [pc]	JA104	3	45	0	-65C to +150C, 10min dwell	500 cyc	MSL3 @ 260C
Autoclave/PCT [pc]	JA102	3	45	0	121C/100%RH/2atm	96hr	MSL3 @ 260C
Material Analysis	RoHS				Materials meet RoHS requirements. ICP reports on file.		
Datasheet Changes					ML0024 Rev 1.6		
Change Notification					PCN10062		

			SPEC		-40C		0C		25C		70C		85C		Margin to Spec (-I)	Margin to Spec (-C)	Notes
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
READ CYCLE																	
ELQV	1	Chip Enable Access Time		25ns	16.8ns	19.4ns	18.0ns	20.6ns	19.0ns	21.2ns	20.6ns	22.8ns	20.8ns	23.4ns	1.6ns	2.2ns	
AVAVR	2	Read Cycle Time	25ns		14.8ns	17.4ns	16.0ns	18.8ns	16.8ns	19.8ns	18.4ns	22.2ns	18.8ns	23.0ns	2.0ns	2.8ns	
AVQV	3	Address Access Time		25ns	18.2ns	19.6ns	19.8ns	21.0ns	20.8ns	22.0ns	22.0ns	23.6ns	22.4ns	24.0ns	1.0ns	1.4ns	
GLOV	4	Output Enable to Data Valid		12ns	6.8ns	9.0ns	7.4ns	9.6ns	7.8ns	10.0ns	8.6ns	10.8ns	8.6ns	11.0ns	1.0ns	1.4ns	
AXQX	5	Output Hold after Address Change	3ns		9.0ns	14.8ns	9.4ns	15.4ns	10.0ns	16.2ns	10.6ns	16.8ns	10.8ns	17.0ns	6.0ns	6.4ns	
ELQX	6	Chip Enable to Output Active	3ns		16.6ns	20.4ns	18.2ns	22.2ns	19.0ns	23.0ns	20.2ns	25.2ns	20.8ns	25.8ns	13.6ns	15.2ns	
EHQZ	7	Chip Enable to Output Inactive		10ns	9.0ns	13.2ns	9.6ns	14.0ns	10.0ns	14.0ns	10.8ns	15.6ns	11.0ns	16.0ns	-6.0ns	-5.6ns	Measurement Issue
GLQX	8	Output Enable to Output Active	0ns		6.8ns	10.0ns	7.4ns	11.0ns	8.0ns	11.6ns	8.6ns	12.8ns	8.8ns	13.8ns	6.8ns	7.4ns	
GHQZ	9	Output Enable to Output Inactive		10ns	9.0ns	13.0ns	9.4ns	14.0ns	9.8ns	14.4ns	10.4ns	15.4ns	10.6ns	15.8ns	-5.8ns	-5.4ns	Measurement Issue
ELICCH	10	Chip Enable to Power Active	0ns														
EHICCL	11	ChipDisable to Power Standby		25ns													
WRITE CYCLE #1 (W/ Controlled)																	
AVAV	12	Write Cycle Time	25ns														
WLWH	13	Write Pulse Width	20ns		5.8ns	7.6ns	6.2ns	8.6ns	6.4ns	8.8ns	6.8ns	8.8ns	7.0ns	9.0ns	11.0ns	11.2ns	
ELWH	14	Chip Enable to End of Write	20ns		5.0ns	7.0ns	5.4ns	8.0ns	5.8ns	8.2ns	6.2ns	8.4ns	6.4ns	8.6ns	11.4ns	11.6ns	
DVWH	15	Data Set-up to End of Write	10ns		5.8ns	7.2ns	6.2ns	8.2ns	6.6ns	8.4ns	7.0ns	8.4ns	7.2ns	8.4ns	1.6ns	1.6ns	
WHDX	16	Data Hold after End of Write	0ns		-2.0ns	-1.6ns	-2.2ns	-1.8ns	-2.2ns	-1.8ns	-2.4ns	-2.0ns	-2.4ns	-2.2ns	1.6ns	1.8ns	
AVWH	17	Address Set-up to End of Write	20ns		4.8ns	5.4ns	5.2ns	6.0ns	5.8ns	6.0ns	6.2ns	6.8ns	6.4ns	8.8ns	13.2ns	13.2ns	
AVWL	18	Address Set-up to Start of Write	0ns		-2.4ns	-1.4ns	-2.4ns	-1.6ns	-2.6ns	-1.8ns	-2.8ns	-1.8ns	-3.0ns	-2.0ns	1.4ns	1.6ns	
WHAX	19	Address Hold after End of Write	0ns		-2.2ns	-1.4ns	-2.2ns	-1.6ns	-2.2ns	-1.6ns	-2.2ns	-1.6ns	-2.4ns	-1.8ns	1.4ns	1.6ns	
WLQZ	20	Write Enable to Output Disable		10ns	8.6ns	13.8ns	9.0ns	14.6ns	9.4ns	15.4ns	10.2ns	16.0ns	10.4ns	16.4ns	-6.4ns	-6.0ns	Measurement Issue
WHQX	21	Output Active after End of Write	3ns		18.8ns	21.6ns	20.2ns	23.2ns	21.0ns	24.4ns	22.6ns	26.6ns	23.2ns	27.4ns	15.8ns	17.2ns	
WRITE CYCLE #2 (E/ Controlled)																	
AVAV	12	Write Cycle Time	25ns														
WLEH	13	Write Pulse Width	20ns		4.0ns	5.2ns	4.4ns	5.4ns	4.8ns	5.8ns	5.0ns	6.4ns	5.4ns	6.6ns	13.4ns	13.6ns	
ELEH	14	Chip Enable to End of Write	20ns		5.8ns	7.8ns	6.2ns	8.6ns	6.6ns	8.8ns	7.0ns	8.8ns	7.2ns	9.0ns	11.0ns	11.2ns	
DVEH	15	Data Set-up to End of Write	10ns		5.2ns	6.8ns	5.8ns	7.8ns	6.0ns	7.8ns	6.6ns	8.2ns	6.2ns	8.2ns	1.8ns	1.8ns	
EHDH	16	Data Hold after End of Write	0ns		-1.6ns	-1.2ns	-1.8ns	-1.4ns	-1.8ns	-1.6ns	-2.0ns	-1.6ns	-2.2ns	-1.8ns	1.2ns	1.4ns	
AVEH	17	Address Set-up to End of Write	20ns		4.6ns	5.0ns	5.0ns	5.4ns	5.2ns	5.8ns	5.8ns	6.4ns	6.0ns	6.6ns	13.4ns	13.6ns	
AVEL	18	Address Set-up to Start of Write	0ns		-2.6ns	-1.8ns	-2.8ns	-2.0ns	-3.0ns	-2.2ns	-3.2ns	-2.2ns	-3.2ns	-2.4ns	1.8ns	2.0ns	
EHAX	19	Address Hold after End of Write	0ns		-1.8ns	-1.2ns	-1.8ns	-1.2ns	-2.0ns	-1.4ns	-2.0ns	-1.4ns	-2.2ns	-1.4ns	1.2ns	1.2ns	
NV PARAMETERS																	
AVAV	26	CE Controlled Initiation Cycle Time (Soft Seq)	25ns														
AVAV	26	OE Controlled Initiation Cycle Time (Soft Seq)	25ns														
AVELN	27	Address Set-up to Start of Write (Soft Seq)	0ns		-5.4ns	-4.2ns	-5.8ns	-4.4ns	-6.0ns	-4.6ns	-6.2ns	-4.8ns	-6.4ns	0.0ns	0.0ns	4.4ns	
AVGL	27	Address Set-up to Start of OE (Soft Seq)	0ns		-5.4ns	-4.2ns	-5.6ns	-4.4ns	-6.0ns	-4.6ns	-6.2ns	-4.8ns	-6.6ns	0.0ns	0.0ns	4.4ns	
ELEHN	28	Chip Enable to End of Write (Soft Seq)	20ns		3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	0.0ns	16.8ns	16.8ns	
GLGH	28	Output Enable Pulse Width (Soft Seq)	20ns		2.4ns	3.0ns	2.4ns	3.0ns	2.4ns	3.0ns	2.6ns	3.0ns	2.6ns	0.0ns	17.0ns	17.0ns	
ELAX	29	Address Hold after CE low (Soft Seq)	0ns		7.2ns	7.8ns	7.6ns	8.2ns	7.8ns	8.6ns	8.4ns	9.2ns	8.6ns	0.0ns	0.0ns	7.6ns	
GLAX	29	Address Hold after OE low (Soft Seq)	0ns		7.2ns	7.8ns	7.6ns	8.2ns	7.8ns	8.6ns	8.4ns	9.2ns	8.6ns	0.0ns	0.0ns	7.6ns	
ELQXS	23	Store Cycle Duration (Soft Seq)		15ms	11.6ms	13.3ms	10.1ms	11.1ms	9.4ms	10.1ms	8.3ms	8.9ms	8.0ms	8.5ms	1.7ms	3.9ms	
ELQXR	30	Recall Cycle Duration (Soft Seq)		50us	35.2us	40.4us	30.7us	33.8us	28.4us	30.6us	25.2us	26.9us	24.3us	25.9us	9.6us	16.2us	
VCCRIS	25	VCC Rise Time	150us														
DELAY	31	Time to Complete SRAM Cycle	1us														
HLHH	32	Hardware Store Pulse Width	15ns		3.8ns	5.2ns	3.8ns	5.4ns	3.8ns	5.6ns	4.2ns	6.0ns	4.2ns	0.0ns	9.0ns	9.0ns	
HLBL	33	Hardware Store Low to Store Busy		300ns													
DC CHARACTERISTICS																	
ICC1		Average Vcc Current @ AVAV=25ns		70mA	36.2mA	46.3mA	36.2mA	44.2mA	36.4mA	43.4mA	36.2mA	41.6mA	36.1mA	41.1mA	23.7mA	25.8mA	
ICC2		Average Vcc Current During Store		3mA	1.2mA	2.1mA	1.3mA	1.5mA	1.5mA	1.7mA	1.8mA	2.0mA	2.0mA	2.3mA	0.8mA	1.0mA	
ICC3		Average Vcc Current @200ns		10mA	5.2mA	5.6mA	5.4mA	6.4mA	5.5mA	6.4mA	5.6mA	6.2mA	5.7mA	6.6mA	3.4mA	3.6mA	
ICC4		Average Vcap Current during Autostore		3mA													
ISB		Vcc Standby Current		3mA	1.1mA	1.7mA	1.3mA	1.8mA	1.3mA	2.0mA	1.5mA	2.0mA	1.5mA	2.1mA	0.9mA	1.0mA	
ILKG		Input Leakage Current	-1uA	1uA													
IOLKG		Off-State Output Leakage Current	-1uA	1uA													
VIH		Input Logic "1" Level	2.0V		1.4V	1.9V	1.2V	1.9V	1.1V	1.9V	1.1V	1.8V	1.1V	1.8V	0.1V	0.1V	
VIL		Input Logic "0" Level		0.8V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	0.2V	0.2V	
VOH		Output Logic "1" Voltage	2.4V		2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	0.2V	0.2V	
VOL		Output Logic "0" Voltage		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VOLBU		Logic "0" Voltage on HSB1 Output		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VSWITCH	24	Autostore Trigger Point		2.65V	2.46V	2.56V	2.48V	2.57V	2.48V	2.59V	2.48V	2.59V	2.48V	2.51V	0.06V	0.06V	

			SPEC		-40C		0C		25C		70C		85C		Margin to Spec (-I)	Margin to Spec (-C)	Notes
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
READ CYCLE																	
ELQV	1	Chip Enable Access Time		45ns	26.8ns	30.6ns	29.0ns	33.0ns	30.8ns	35.0ns	32.6ns	37.4ns	33.4ns	38.2ns	6.8ns	7.6ns	
AVAVR	2	Read Cycle Time	45ns		24.2ns	27.4ns	26.2ns	29.8ns	28.4ns	32.0ns	30.2ns	34.2ns	31.0ns	35.4ns	9.6ns	10.8ns	
AVQV	3	Address Access Time		45ns	28.0ns	31.0ns	30.2ns	33.6ns	33.0ns	35.8ns	34.4ns	37.8ns	35.2ns	39.0ns	6.0ns	7.2ns	
GLOV	4	Output Enable to Data Valid		20ns	6.6ns	9.0ns	7.2ns	9.8ns	7.8ns	10.6ns	8.4ns	11.0ns	8.6ns	11.4ns	8.6ns	9.0ns	
AXQX	5	Output Hold after Address Change	3ns		9.0ns	14.8ns	9.4ns	15.6ns	10.2ns	16.4ns	10.4ns	16.8ns	10.8ns	17.0ns	6.0ns	6.4ns	
ELQX	6	Chip Enable to Output Active	3ns		27.0ns	31.6ns	29.0ns	34.2ns	31.4ns	37.2ns	32.6ns	39.6ns	33.6ns	40.8ns	24.0ns	26.0ns	
EHQZ	7	Chip Enable to Output Inactive		15ns	9.0ns	13.4ns	9.6ns	14.4ns	10.2ns	15.2ns	10.4ns	16.0ns	10.8ns	16.0ns	-1.0ns	-1.0ns	Measurement Issue
GLOX	8	Output Enable to Output Active	0ns		6.8ns	10.0ns	7.4ns	11.0ns	8.2ns	12.4ns	8.4ns	13.2ns	8.8ns	13.8ns	6.8ns	7.4ns	
GHQZ	9	Output Enable to Output Inactive		15ns	8.8ns	13.2ns	9.4ns	13.8ns	10.0ns	15.2ns	10.4ns	15.8ns	10.6ns	15.8ns	-0.8ns	-0.8ns	Measurement Issue
ELICCH	10	Chip Enable to Power Active	0ns														
EHICCL	11	ChipDisable to Power Standby		45ns													
WRITE CYCLE #1 (W/ Controlled)																	
AVAV	12	Write Cycle Time	45ns														
WLWH	13	Write Pulse Width	30ns		5.8ns	6.6ns	6.2ns	7.2ns	6.6ns	8.0ns	6.8ns	8.0ns	7.0ns	8.2ns	21.8ns	22.0ns	
ELWH	14	Chip Enable to End of Write	30ns		5.0ns	6.4ns	5.4ns	6.6ns	6.0ns	7.2ns	6.2ns	7.6ns	6.4ns	7.8ns	22.2ns	22.4ns	
DVWH	15	Data Set-up to End of Write	15ns		5.8ns	6.6ns	6.2ns	7.0ns	6.6ns	7.6ns	6.8ns	7.8ns	7.0ns	8.2ns	6.8ns	7.2ns	
WHDX	16	Data Hold after End of Write	0ns		-2.2ns	-1.8ns	-2.2ns	-2.0ns	-2.4ns	-2.2ns	-2.6ns	-2.2ns	-2.6ns	-2.2ns	1.8ns	2.0ns	
AVWH	17	Address Set-up to End of Write	30ns		4.6ns	5.4ns	5.2ns	6.0ns	5.8ns	6.6ns	6.0ns	7.0ns	6.4ns	7.2ns	22.8ns	23.0ns	
AVWL	18	Address Set-up to Start of Write	0ns		-2.4ns	-1.6ns	-2.6ns	-1.8ns	-2.8ns	-1.8ns	-3.0ns	-2.0ns	-3.0ns	-2.0ns	1.6ns	1.8ns	
WHAX	19	Address Hold after End of Write	0ns		-2.2ns	-1.4ns	-2.2ns	-1.4ns	-2.4ns	-1.6ns	-2.4ns	-1.6ns	-2.4ns	-1.6ns	1.4ns	1.4ns	
WLQZ	20	Write Enable to Output Disable		15ns	8.2ns	13.8ns	9.0ns	14.4ns	9.6ns	15.4ns	9.8ns	16.2ns	10.2ns	16.2ns	-1.2ns	-1.2ns	Measurement Issue
WHQX	21	Output Active after End of Write	3ns		28.4ns	32.2ns	30.4ns	34.8ns	32.6ns	37.6ns	34.2ns	40.0ns	35.0ns	41.2ns	25.4ns	27.4ns	
WRITE CYCLE #2 (E/ Controlled)																	
AVAV	12	Write Cycle Time	45ns														
WLEH	13	Write Pulse Width	30ns		3.8ns	5.0ns	4.4ns	5.4ns	4.8ns	6.2ns	5.0ns	6.4ns	5.4ns	6.6ns	23.4ns	23.6ns	
ELEH	14	Chip Enable to End of Write	30ns		5.8ns	7.0ns	6.2ns	7.4ns	6.6ns	7.8ns	6.8ns	8.0ns	7.2ns	8.0ns	22.0ns	22.0ns	
DVEH	15	Data Set-up to End of Write	15ns		5.2ns	5.8ns	5.4ns	6.4ns	6.2ns	6.8ns	6.6ns	7.0ns	6.6ns	7.4ns	7.6ns	8.0ns	
EHDH	16	Data Hold after End of Write	0ns		-1.6ns	-1.2ns	-1.8ns	-1.4ns	-2.0ns	-1.6ns	-2.2ns	-1.8ns	-2.2ns	-1.8ns	1.2ns	1.4ns	
AVEH	17	Address Set-up to End of Write	30ns		4.2ns	5.0ns	4.6ns	5.4ns	5.4ns	6.0ns	5.8ns	6.4ns	6.0ns	6.6ns	23.4ns	23.6ns	
AVEL	18	Address Set-up to Start of Write	0ns		-2.6ns	-2.0ns	-2.8ns	-2.0ns	-3.0ns	-2.2ns	-3.2ns	-2.4ns	-3.4ns	-2.4ns	2.0ns	2.0ns	
EHAX	19	Address Hold after End of Write	0ns		-1.8ns	-1.0ns	-1.8ns	-1.2ns	-2.0ns	-1.2ns	-2.0ns	-1.2ns	-2.2ns	-1.2ns	1.0ns	1.2ns	
NV PARAMETERS																	
AVAV	26	CE Controlled Initiation Cycle Time (Soft Seq)	45ns														
AVAV	26	OE Controlled Initiation Cycle Time (Soft Seq)	45ns														
AVELN	27	Address Set-up to Start of Write (Soft Seq)	0ns		-5.4ns	-4.0ns	-5.8ns	-4.4ns	-6.0ns	-4.6ns	-6.2ns	-4.8ns	-6.4ns	0.0ns	0.0ns	4.4ns	
AVGL	27	Address Set-up to Start of OE (Soft Seq)	0ns		-5.4ns	-4.0ns	-5.6ns	-4.2ns	-6.0ns	-4.6ns	-6.2ns	-4.8ns	-6.4ns	0.0ns	0.0ns	4.2ns	
ELEHN	28	Chip Enable to End of Write (Soft Seq)	30ns		3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	0.0ns	26.8ns	26.8ns	
GLGH	28	Output Enable Pulse Width (Soft Seq)	30ns		2.4ns	3.0ns	2.4ns	3.0ns	2.6ns	3.0ns	2.6ns	3.0ns	2.6ns	0.0ns	27.0ns	27.0ns	
ELAX	29	Address Hold after CE low (Soft Seq)	0ns		7.2ns	7.8ns	7.6ns	8.2ns	8.0ns	8.8ns	8.4ns	9.0ns	8.6ns	0.0ns	0.0ns	7.6ns	
GLAX	29	Address Hold after OE low (Soft Seq)	0ns		7.2ns	7.8ns	7.6ns	8.2ns	8.0ns	8.8ns	8.4ns	9.2ns	8.6ns	0.0ns	0.0ns	7.6ns	
ELQXS	23	Store Cycle Duration (Soft Seq)		15ms	12.5ms	13.2ms	10.8ms	11.1ms	9.3ms	9.6ms	8.6ms	8.2ms	8.4ms	1.8ms	3.9ms		
ELQXR	30	Recall Cycle Duration (Soft Seq)		50us	37.9us	40.0us	32.7us	33.7us	28.2us	29.2us	26.0us	26.8us	24.9us	25.6us	10.0us	16.3us	
VCCRIS	25	VCC Rise Time	150us														
DELAY	31	Time to Complete SRAM Cycle	1us														
HLHH	32	Hardware Store Pulse Width	15ns		3.8ns	5.2ns	3.8ns	5.4ns	4.0ns	5.8ns	4.2ns	6.0ns	4.2ns	0.0ns	9.0ns	9.0ns	
HLBL	33	Hardware Store Low to Store Busy		300ns													
DC CHARACTERISTICS																	
ICC1		Average Vcc Current @ AVAV=45ns		50mA	30.0mA	41.8mA	30.2mA	39.5mA	30.2mA	37.4mA	30.0mA	36.6mA	30.0mA	36.0mA	8.2mA	10.5mA	
ICC2		Average Vcc Current During Store		3mA	1.1mA	1.5mA	1.3mA	1.9mA	1.5mA	1.7mA	1.7mA	2.0mA	1.9mA	2.2mA	0.8mA	1.0mA	
ICC3		Average Vcc Current @200ns		10mA	7.0mA	7.7mA	7.4mA	7.8mA	7.7mA	8.3mA	7.6mA	8.7mA	7.9mA	8.8mA	1.2mA	1.3mA	
ICC4		Average Vcap Current during Autostore		3mA													
ISB		Vcc Standby Current		3mA	1.1mA	1.6mA	1.2mA	1.8mA	1.3mA	1.9mA	1.4mA	2.0mA	1.5mA	2.1mA	0.9mA	1.0mA	
ILKG		Input Leakage Current		-1uA	1uA												
IOLKG		Off-State Output Leakage Current		-1uA	1uA												
VIH		Input Logic "1" Level		2.0V	1.5V	1.9V	1.4V	1.9V	1.3V	1.9V	1.2V	1.9V	1.3V	1.8V	0.1V	0.1V	
VIL		Input Logic "0" Level		0.8V	1.1V	1.4V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	1.0V	1.2V	0.2V	0.2V	
VOH		Output Logic "1" Voltage		2.4V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	0.2V	0.2V	
VOL		Output Logic "0" Voltage		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VOLBU		Logic "0" Voltage on HSB1 Output		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VSWITCH	24	Autostore Trigger Point		2.65V	2.48V	2.59V	2.48V	2.59V	2.49V	2.60V	2.49V	2.65V	2.49V	2.69V	-0.04V	0.00V	