



# Product Qualification Report

## Product Qualification Report

### **STK14D88 Revision B**

Issue 00 Dated 07 July 2006

Ref PCN10038 Device Revision Change

#### **SUMMARY**

The design and process for this product were modified to resolve number of issues found in the initial product release. Simtek PCN 10038, attached, outlines these changes. The datasheet characterization data for 25, 35 and 45ns product over industrial temp range is in Table I. The qualification data for the new revision is in Table II.

#### **PRODUCT AFFECTED**

STK14D88 1M nvSRAM

All package types

Commercial and Industrial grades

#### **NEW PRODUCT DESIGN REV ID**

Product built using the new design and process revisions will be marked "**Simtek B**" on the first line of the topside mark.



# Qualification Status Report

## Table II Qualification Lifetest Report

[Lifetest samples from 3 separate wafer fab lots]

Stress	Method	# of Lots	SS/Lot	C=	Conditions	Duration	Result
High Temp Operating Life	JA108	3	77	0	140C External Vcc 3.6V Internal regulated 2.4V	352hr	231/0
HTOL Variables <sup>[1]</sup>	JA108	3	15	0	140C External Vcc 3.6V Internal regulated 2.4V	352hr	45/0
Endurance - Softstore	JA117	3	77	0	25C <sup>[2]</sup>	500K softstore	228/0
Endurance - Autostore <sup>[3]</sup>	JA117	3	77	0	25C <sup>[2]</sup>	500K autostore	229/0
High Temp Retention Bake	JA103	1	77	0	200C	96hr <sup>[4]</sup>	
STK14D88 1M nvSRAM	JA108	1	77	0			
ESD - HBM	JA114	1	9	0			Pass @ '2KV
ESD - CDM	JC101	1	3	0			Pass @ 500V
Latch-Up	JESD78	1	6	0			Pass @ +/-200mA/85C
Datasheet Churn	STK	3	15	Cpk>1.33			Meets datasheet
Early Life Failure Rate	JESD74	3	1K	C=1	125C External Vcc 3.6V, Internal regulated 2.4V	48hr	Ongoing <sup>[5]</sup>
Physical Dimensions	JB105	1	15	Cpk>1.66	Per package outline		Meets spec
Bond Pull Strength	M2011	1		Cpk>1.33			Meets spec
Die Shear	M2019	1	5	0			
Preconditioning	JA113				Per J-STD-020 and JEDEC22-A113		
MSL Classification	JS020	3	22	0	Per J-STD-020 for lead-free 260C peak reflow		MSL3 @ 260C
Temperature Cycling [pc]	JA104	3	45	0	-65C to +150C, 10min dwell	500 cyc	MSL3 @ 260C
Autoclave/PCT [pc]	JA102	3	45	0	96hr 121C 2atm 100%RH	96hr	MSL3 @ 260C
Material Analysis	RoHS				ICP Reports & Materials DS Documentation on file		
Change Notification							PCN10038

### Notes for Table II

1. HTOL variables criteria <10% variation and within datasheet after 1Khr 125C equivalent.
2. Store cycle endurance characterized at temp.
3. Autostore cycling based on power cycling forcing autostore and recall at each cycle
4. 96hr @ 200C is equivalent to 1Khr @ 150C and approx 20years @ 55C
5. Early Life Failure Rate not required for qualification release. Completion within 6 months of production release.

STK14D88 Rev B 25ns Characterization Report

			SPEC		-40C		0C		25C		70C		85C		Margin to Spec (-I)	Margin to Spec (-C)	Notes
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
<b>READ CYCLE</b>																	
ELQV	1	Chip Enable Access Time		25ns	15.6ns	18.4ns	16.8ns	19.8ns	17.4ns	20.6ns	18.6ns	21.8ns	19.2ns	22.4ns	2.6ns	3.2ns	
AVAVR	2	Read Cycle Time	25ns		15.2ns	18.0ns	16.8ns	19.2ns	17.2ns	20.0ns	18.4ns	21.4ns	19.2ns	22.2ns	2.8ns	3.6ns	
AVQV	3	Address Access Time		25ns	17.6ns	19.6ns	19.0ns	21.0ns	19.8ns	21.8ns	21.2ns	23.2ns	21.6ns	24.0ns	1.0ns	1.8ns	
GLQV	4	Output Enable to Data Valid		12ns	6.0ns	8.2ns	6.6ns	8.8ns	6.8ns	9.2ns	7.2ns	9.8ns	7.6ns	10.2ns	1.8ns	2.2ns	
AXQX	5	Output Hold after Address Change	3ns		8.6ns	14.4ns	9.2ns	15.2ns	9.4ns	15.6ns	10.0ns	16.0ns	10.2ns	16.4ns	5.6ns	6.2ns	
ELQX	6	Chip Enable to Output Active	3ns		16.2ns	20.2ns	17.4ns	21.8ns	18.2ns	23.0ns	19.4ns	25.0ns	19.6ns	26.0ns	13.2ns	14.4ns	
EHQZ	7	Chip Enable to Output Inactive		10ns		6.0ns		6.5ns		7.5ns		7.5ns		8.0ns	2.0ns	2.5ns	
GLQX	8	Output Enable to Output Active	0ns		6.8ns	10.0ns	7.4ns	11.0ns	7.6ns	11.8ns	8.2ns	13.0ns	8.4ns	13.8ns	6.8ns	7.4ns	
GHQZ	9	Output Enable to Output Inactive		10ns		6.5ns		7.0ns		7.5ns		7.5ns		8.5ns	1.5ns	2.5ns	
ELICCH	10	Chip Enable to Power Active	0ns														
EHICCL	11	ChipDisable to Power Standby		25ns													
<b>WRITE CYCLE #1 (W/ Controlled)</b>																	
AVAV	12	Write Cycle Time	25ns														
WLWH	13	Write Pulse Width	20ns		5.8ns	6.8ns	6.0ns	7.4ns	6.2ns	8.0ns	6.6ns	8.2ns	6.8ns	8.4ns	11.6ns	11.8ns	
ELWH	14	Chip Enable to End of Write	20ns		4.8ns	6.2ns	5.4ns	6.6ns	5.6ns	7.0ns	6.0ns	7.4ns	6.2ns	7.6ns	12.4ns	12.6ns	
DVWH	15	Data Set-up to End of Write	10ns		5.4ns	6.6ns	5.8ns	7.0ns	6.0ns	7.2ns	6.6ns	7.8ns	6.6ns	8.0ns	2.0ns	2.2ns	
WHDH	16	Data Hold after End of Write	0ns		-4.2ns	-3.4ns	-4.6ns	-3.6ns	-4.8ns	-3.8ns	-5.2ns	-4.0ns	-5.4ns	-4.0ns	3.4ns	3.6ns	
AVWH	17	Address Set-up to End of Write	20ns		4.6ns	6.0ns	5.2ns	6.4ns	5.4ns	6.6ns	6.0ns	7.0ns	6.2ns	7.2ns	12.8ns	13.0ns	
AVWL	18	Address Set-up to Start of Write	0ns		-2.6ns	-1.6ns	-2.8ns	-1.6ns	-2.8ns	-1.8ns	-3.0ns	-1.8ns	-3.2ns	-2.0ns	1.6ns	1.6ns	
WHAX	19	Address Hold after End of Write	0ns		-2.2ns	-1.4ns	-2.2ns	-1.4ns	-2.2ns	-1.6ns	-2.4ns	-1.6ns	-2.4ns	-1.6ns	1.4ns	1.4ns	
WLQZ	20	Write Enable to Output Disable		10ns		7.5ns		8.5ns		9.0ns		9.5ns		9.5ns	0.5ns	0.5ns	
WHQX	21	Output Active after End of Write	3ns		18.2ns	21.4ns	19.4ns	23.0ns	20.2ns	24.6ns	21.4ns	26.2ns	22.2ns	27.2ns	15.2ns	16.4ns	
<b>WRITE CYCLE #2 (E/ Controlled)</b>																	
AVAV	12	Write Cycle Time	25ns														
WLEH	13	Write Pulse Width	20ns		3.8ns	5.4ns	4.2ns	5.8ns	4.6ns	6.2ns	5.0ns	6.6ns	5.0ns	7.0ns	13.0ns	13.4ns	
ELEH	14	Chip Enable to End of Write	20ns		5.6ns	6.8ns	6.0ns	7.4ns	6.2ns	7.6ns	6.6ns	8.0ns	6.8ns	8.2ns	11.8ns	12.0ns	
DVEH	15	Data Set-up to End of Write	10ns		5.0ns	5.4ns	5.2ns	6.0ns	5.6ns	6.4ns	6.2ns	6.6ns	6.2ns	6.8ns	3.2ns	3.4ns	
EHDH	16	Data Hold after End of Write	0ns		-3.6ns	-3.0ns	-4.0ns	-3.2ns	-4.4ns	-3.4ns	-4.6ns	-3.6ns	-4.8ns	-3.8ns	3.0ns	3.2ns	
AVEH	17	Address Set-up to End of Write	20ns		4.4ns	5.4ns	4.8ns	5.8ns	5.2ns	6.0ns	5.8ns	6.4ns	6.0ns	6.6ns	13.4ns	13.6ns	
AVEL	18	Address Set-up to Start of Write	0ns		-2.8ns	-1.8ns	-3.0ns	-2.0ns	-3.2ns	-2.0ns	-3.2ns	-2.0ns	-3.4ns	-2.2ns	1.8ns	2.0ns	
EHAX	19	Address Hold after End of Write	0ns		-1.8ns	-1.0ns	-1.8ns	-1.2ns	-2.0ns	-1.2ns	-2.0ns	-1.2ns	-2.2ns	-1.2ns	1.0ns	1.2ns	
<b>NV PARAMETERS</b>																	
AVAV	26	CE Controlled Initiation Cycle Time (Soft Seq)	25ns														
AVAV	26	OE Controlled Initiation Cycle Time (Soft Seq)	25ns														
AVELN	27	Address Set-up to Start of Write (Soft Seq)	0ns		-5.4ns	-4.0ns	-5.6ns	-4.2ns	-6.0ns	-4.2ns	-6.0ns	-4.6ns	-6.2ns	-4.6ns	4.0ns	4.2ns	
AVGL	27	Address Set-up to Start of OE (Soft Seq)	0ns		-5.4ns	-4.0ns	-5.6ns	-4.2ns	-6.0ns	-4.2ns	-6.0ns	-4.6ns	-6.2ns	-4.6ns	4.0ns	4.2ns	
ELEHN	28	Chip Enable to End of Write (Soft Seq)	20ns		3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	16.8ns	16.8ns	
GLGH	28	Output Enable Pulse Width (Soft Seq)	20ns		2.4ns	3.0ns	2.4ns	3.0ns	2.4ns	3.0ns	2.4ns	3.0ns	2.6ns	3.0ns	17.0ns	17.0ns	
ELAX	29	Address Hold after CE low (Soft Seq)	0ns		7.0ns	7.8ns	7.2ns	8.2ns	7.6ns	8.6ns	7.8ns	9.0ns	8.0ns	9.2ns	7.0ns	7.2ns	
GLAX	29	Address Hold after OE low (Soft Seq)	0ns		7.0ns	7.8ns	7.2ns	8.2ns	7.6ns	8.6ns	8.0ns	9.0ns	8.2ns	9.2ns	7.0ns	7.2ns	
ELQXS	23	Store Cycle Duration (Soft Seq)		15ms	12.6ms	13.7ms	10.8ms	11.3ms	9.9ms	10.2ms	8.7ms	8.9ms	8.2ms	8.5ms	1.3ms	3.7ms	
ELQXR	30	Recall Cycle Duration (Soft Seq)		50us	38.1us	41.6us	32.8us	34.3us	29.9us	30.8us	26.2us	26.8us	24.9us	25.7us	8.4us	15.7us	
VCCRISE	25	VCC Rise Time	150us														
DELAY	31	Time to Complete SRAM Cycle	1us														
HLHH	32	Hardware Store Pulse Width	15ns		3.6ns	5.0ns	3.6ns	5.2ns	3.8ns	5.6ns	3.8ns	5.8ns	3.8ns	6.0ns	9.0ns	9.2ns	
HLBL	33	Hardware Store Low to Store Busy		300ns													
<b>DC CHARACTERISTICS</b>																	
ICC1		Average Vcc Current @ AVAV=25ns		70mA	36.6mA	46.4mA	36.7mA	45.0mA	36.7mA	44.2mA	36.7mA	42.8mA	36.8mA	42.3mA	23.6mA	25.0mA	
ICC2		Average Vcc Current During Store		3mA	1.2mA	2.1mA	1.3mA	1.5mA	1.5mA	1.6mA	1.8mA	2.0mA	2.0mA	2.2mA	0.8mA	1.1mA	
ICC3		Average Vcc Current @200ns		10mA	5.1mA	5.5mA	5.3mA	5.9mA	5.4mA	6.2mA	5.7mA	6.3mA	5.8mA	6.7mA	3.3mA	3.7mA	
ICC4		Average Vcap Current during Autostore		3mA													
ISB		Vcc Standby Current		3mA	1.1mA	1.7mA	1.2mA	1.8mA	1.3mA	1.8mA	1.4mA	2.0mA	1.6mA	2.1mA	0.9mA	1.0mA	
ILKG		Input Leakage Current	-1uA	1uA													
IOLKG		Off-State Output Leakage Current	-1uA	1uA													
VIH		Input Logic "1" Level	2.2V		1.4V	1.9V	1.1V	1.9V	1.1V	1.9V	1.1V	1.8V	1.1V	1.8V	0.3V	0.3V	
VIL		Input Logic "0" Level		0.8V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	0.2V	0.2V	
VOH		Output Logic "1" Voltage	2.4V		2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	0.2V	0.2V	
VOL		Output Logic "0" Voltage		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VOLBU		Logic "0" Voltage on HSB\ Output		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VSWITCH	24	Autostore Trigger Point		2.65V		2.48V		2.49V		2.58V		2.60V		2.59V			

STK14D88 Rev B 35ns Characterization Report

			SPEC		-40C		0C		25C		70C		85C		Margin to Spec (-I)	Margin to Spec (-C)	Notes
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
<b>READ CYCLE</b>																	
ELQV	1	Chip Enable Access Time		35ns	16.4ns	20.4ns	17.8ns	21.6ns	18.6ns	23.4ns	19.8ns	24.4ns	20.0ns	25.4ns	9.6ns	10.6ns	
AVAVR	2	Read Cycle Time	35ns		14.2ns	18.0ns	16.0ns	21.6ns	17.2ns	21.0ns	18.4ns	22.4ns	19.2ns	23.2ns	11.8ns	12.6ns	
AVQV	3	Address Access Time		35ns	18.2ns	20.0ns	19.8ns	21.4ns	21.0ns	22.6ns	22.0ns	24.0ns	22.4ns	24.6ns	10.4ns	11.0ns	
GLQV	4	Output Enable to Data Valid		15ns	6.0ns	8.4ns	6.6ns	9.0ns	7.2ns	9.4ns	7.4ns	10.0ns	7.8ns	10.4ns	4.6ns	5.0ns	
AXQX	5	Output Hold after Address Change	3ns		8.8ns	14.4ns	9.2ns	15.2ns	10.0ns	15.8ns	10.4ns	16.2ns	10.6ns	16.6ns	5.8ns	6.2ns	
ELQX	6	Chip Enable to Output Active	3ns		16.6ns	20.6ns	18.0ns	22.4ns	19.4ns	24.0ns	20.2ns	25.6ns	20.6ns	26.6ns	13.6ns	15.0ns	
EHQZ	7	Chip Enable to Output Inactive		13ns		8.7ns		9.0ns		9.5ns		9.5ns		10.9ns	2.1ns	3.5ns	
GLQX	8	Output Enable to Output Active	0ns		6.8ns	10.0ns	7.4ns	11.0ns	8.0ns	12.0ns	8.4ns	13.2ns	8.8ns	14.0ns	6.8ns	7.4ns	
GHQZ	9	Output Enable to Output Inactive		13ns		9.1ns		9.5ns		10.1ns		10.2ns		11.3ns	1.7ns	2.8ns	
ELICCH	10	Chip Enable to Power Active	0ns														
EHICCL	11	ChipDisable to Power Standby		35ns													
<b>WRITE CYCLE #1 (W/ Controlled)</b>																	
AVAV	12	Write Cycle Time	35ns														
WLWH	13	Write Pulse Width	25ns		5.8ns	6.8ns	6.2ns	7.2ns	6.6ns	7.8ns	6.8ns	8.0ns	6.8ns	8.2ns	16.8ns	17.0ns	
ELWH	14	Chip Enable to End of Write	25ns		5.0ns	6.4ns	5.4ns	6.8ns	5.8ns	7.2ns	6.2ns	7.4ns	6.2ns	7.6ns	17.4ns	17.6ns	
DVWH	15	Data Set-up to End of Write	12ns		5.8ns	6.8ns	6.0ns	7.0ns	6.6ns	7.4ns	6.8ns	7.8ns	6.8ns	8.2ns	3.8ns	4.2ns	
WHDX	16	Data Hold after End of Write	0ns		-4.4ns	-3.6ns	-4.8ns	-3.8ns	-5.0ns	-4.0ns	-5.4ns	-4.4ns	-5.6ns	-4.4ns	3.6ns	3.8ns	
AVWH	17	Address Set-up to End of Write	25ns		4.6ns	5.4ns	5.4ns	5.8ns	5.8ns	6.2ns	6.0ns	6.8ns	6.0ns	6.8ns	18.2ns	18.2ns	
AVWL	18	Address Set-up to Start of Write	0ns		-2.4ns	-1.6ns	-2.6ns	-1.6ns	-2.8ns	-1.8ns	-2.8ns	-2.0ns	-3.0ns	-2.0ns	1.6ns	1.6ns	
WHAX	19	Address Hold after End of Write	0ns		-2.2ns	-1.6ns	-2.4ns	-1.6ns	-2.4ns	-1.6ns	-2.4ns	-1.6ns	-2.4ns	-1.6ns	1.6ns	1.6ns	
WLQZ	20	Write Enable to Output Disable		13ns		10.5ns		11.4ns		12.0ns		12.1ns		12.8ns	0.2ns	0.9ns	
WHQX	21	Output Active after End of Write	3ns		18.8ns	21.8ns	20.2ns	23.6ns	21.6ns	25.4ns	22.4ns	27.0ns	23.2ns	28.0ns	15.8ns	17.2ns	
<b>WRITE CYCLE #2 (E/ Controlled)</b>																	
AVAV	12	Write Cycle Time	35ns														
WLEH	13	Write Pulse Width	25ns		4.0ns	5.0ns	4.4ns	5.4ns	4.8ns	6.0ns	5.2ns	6.4ns	5.4ns	6.6ns	18.4ns	18.6ns	
ELEH	14	Chip Enable to End of Write	25ns		5.8ns	6.6ns	6.2ns	7.2ns	6.6ns	7.6ns	6.8ns	8.0ns	7.0ns	8.0ns	17.0ns	17.0ns	
DVEH	15	Data Set-up to End of Write	12ns		5.2ns	5.8ns	5.4ns	6.2ns	6.0ns	6.6ns	6.4ns	6.8ns	6.6ns	7.0ns	5.0ns	5.2ns	
EHDH	16	Data Hold after End of Write	0ns		-3.8ns	-3.2ns	-4.4ns	-3.4ns	-4.6ns	-3.6ns	-5.0ns	-3.8ns	-5.0ns	-3.8ns	3.2ns	3.4ns	
AVEH	17	Address Set-up to End of Write	25ns		4.4ns	5.0ns	5.0ns	5.4ns	5.4ns	5.8ns	5.8ns	6.4ns	5.8ns	6.6ns	18.4ns	18.6ns	
AVEL	18	Address Set-up to Start of Write	0ns		-2.8ns	-1.8ns	-3.0ns	-2.0ns	-3.0ns	-2.2ns	-3.2ns	-2.2ns	-3.4ns	-2.4ns	1.8ns	2.0ns	
EHAX	19	Address Hold after End of Write	0ns		-1.8ns	-1.2ns	-1.8ns	-1.2ns	-2.0ns	-1.2ns	-2.0ns	-1.2ns	-2.0ns	-1.2ns	1.2ns	1.2ns	
<b>NV PARAMETERS</b>																	
AVAV	26	CE Controlled Initiation Cycle Time (Soft Seq)	35ns														
AVAV	26	OE Controlled Initiation Cycle Time (Soft Seq)	35ns														
AVELN	27	Address Set-up to Start of Write (Soft Seq)	0ns		-5.6ns	-4.2ns	-5.8ns	-4.6ns	-6.0ns	-4.6ns	-6.2ns	-4.8ns	-6.6ns	-5.0ns	4.2ns	4.6ns	
AVGL	27	Address Set-up to Start of OE (Soft Seq)	0ns		-5.4ns	-4.2ns	-5.8ns	-4.6ns	-6.0ns	-4.6ns	-6.4ns	-4.8ns	-6.6ns	-5.0ns	4.2ns	4.6ns	
ELEHN	28	Chip Enable to End of Write (Soft Seq)	25ns		3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	21.8ns	21.8ns	
GLGH	28	Output Enable Pulse Width (Soft Seq)	25ns		2.4ns	3.0ns	2.4ns	3.0ns	2.4ns	3.0ns	2.4ns	3.0ns	2.4ns	3.0ns	22.0ns	22.0ns	
ELAX	29	Address Hold after CE low (Soft Seq)	0ns		7.2ns	7.8ns	7.8ns	8.4ns	8.0ns	8.6ns	8.4ns	9.2ns	8.6ns	9.2ns	7.2ns	7.8ns	
GLAX	29	Address Hold after OE low (Soft Seq)	0ns		7.2ns	7.8ns	7.8ns	8.4ns	8.0ns	8.6ns	8.4ns	9.2ns	8.6ns	9.4ns	7.2ns	7.8ns	
ELQXS	23	Store Cycle Duration (Soft Seq)		15ms	11.6ms	13.4ms	10.1ms	11.3ms	9.1ms	9.8ms	8.5ms	9.0ms	8.3ms	8.4ms	1.6ms	3.7ms	
ELQXR	30	Recall Cycle Duration (Soft Seq)		50us	35.1us	40.7us	30.8us	34.3us	27.4us	29.7us	25.7us	27.2us	25.0us	25.4us	9.3us	15.7us	
VCCRIS	25	VCC Rise Time	150us														
DELAY	31	Time to Complete SRAM Cycle	1us														
HLHH	32	Hardware Store Pulse Width	15ns		3.8ns	5.0ns	3.8ns	5.2ns	3.8ns	5.6ns	4.0ns	5.8ns	4.2ns	6.0ns	9.0ns	9.2ns	
HLBL	33	Hardware Store Low to Store Busy		300ns													
<b>DC CHARACTERISTICS</b>																	
ICC1		Average Vcc Current @ AVAV=35ns		60mA	29.5mA	43.6mA	29.4mA	42.0mA	29.6mA	40.5mA	29.6mA	39.4mA	29.4mA	39.1mA	16.4mA	18.0mA	
ICC2		Average Vcc Current During Store		3mA	1.3mA	2.2mA	1.4mA	1.6mA	1.5mA	1.8mA	1.8mA	2.4mA	2.0mA	2.2mA	0.6mA	0.6mA	
ICC3		Average Vcc Current @200ns		10mA	5.2mA	5.7mA	5.4mA	5.9mA	5.6mA	6.1mA	5.7mA	6.3mA	5.8mA	6.8mA	3.2mA	3.7mA	
ICC4		Average Vcap Current during Autostore		3mA													
ISB		Vcc Standby Current		3mA	1.1mA	1.7mA	1.3mA	1.8mA	1.4mA	1.9mA	1.5mA	2.0mA	1.5mA	2.1mA	0.9mA	1.0mA	
ILKG		Input Leakage Current	-1uA	1uA													
IOLKG		Off-State Output Leakage Current	-1uA	1uA													
VIH		Input Logic "1" Level	2.2V		1.5V	1.9V	1.4V	1.9V	1.3V	1.9V	1.2V	1.9V	1.3V	1.9V	0.3V	0.3V	
VIL		Input Logic "0" Level		0.8V	1.1V	1.4V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	0.2V	0.2V	
VOH		Output Logic "1" Voltage	2.4V		2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	0.2V	0.2V	
VOL		Output Logic "0" Voltage		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VOLBU		Logic "0" Voltage on HSB1 Output		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VSWITCH	24	Autostore Trigger Point		2.65V		2.69V		2.57V		2.59V		2.59V		2.59V			

STK14D88 Rev B 45ns Characterization Report

			SPEC		-40C		0C		25C		70C		85C		Margin to Spec (-)	Margin to Spec (-C)	Notes
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
<b>READ CYCLE</b>																	
ELQV	1	Chip Enable Access Time		45ns	26.0ns	29.2ns	28.0ns	31.4ns	29.6ns	34.0ns	31.6ns	35.4ns	32.4ns	36.6ns	8.4ns	9.6ns	
AVAVR	2	Read Cycle Time	45ns		23.2ns	25.8ns	25.2ns	28.2ns	27.4ns	31.0ns	29.2ns	32.4ns	30.0ns	33.4ns	11.6ns	12.6ns	
AVQV	3	Address Access Time		45ns	27.6ns	30.2ns	30.2ns	32.6ns	32.6ns	35.8ns	34.4ns	36.8ns	35.0ns	37.8ns	7.2ns	8.2ns	
GLQV	4	Output Enable to Data Valid		20ns	6.0ns	8.4ns	6.4ns	9.0ns	7.2ns	10.0ns	7.4ns	10.0ns	7.4ns	10.4ns	9.6ns	10.0ns	
AXQX	5	Output Hold after Address Change	3ns		8.6ns	14.4ns	9.2ns	15.0ns	9.8ns	16.0ns	10.2ns	16.2ns	10.4ns	16.4ns	5.6ns	6.2ns	
ELQX	6	Chip Enable to Output Active	3ns		26.8ns	31.0ns	28.8ns	33.6ns	31.2ns	38.4ns	32.6ns	38.8ns	33.4ns	40.0ns	23.8ns	25.8ns	
EHQZ	7	Chip Enable to Output Inactive		15ns		9.8ns		10.2ns		10.9ns		11.6ns		10.9ns	3.4ns	3.4ns	
GLQX	8	Output Enable to Output Active	0ns		6.6ns	10.0ns	7.2ns	11.2ns	7.8ns	13.6ns	8.2ns	13.4ns	8.4ns	14.0ns	6.6ns	7.2ns	
GHQZ	9	Output Enable to Output Inactive		15ns		10.8ns		11.4ns		12.4ns		13.1ns		13.5ns	1.5ns	1.9ns	
ELICCH	10	Chip Enable to Power Active	0ns														
EHICCL	11	ChipDisable to Power Standby		45ns													
<b>WRITE CYCLE #1 (W/ Controlled)</b>																	
AVAV	12	Write Cycle Time	45ns														
WLWH	13	Write Pulse Width	30ns		5.8ns	6.6ns	6.2ns	7.2ns	6.6ns	8.0ns	6.8ns	8.0ns	7.2ns	8.2ns	21.8ns	22.0ns	
ELWH	14	Chip Enable to End of Write	30ns		5.0ns	6.0ns	5.4ns	6.6ns	5.8ns	7.2ns	6.2ns	7.4ns	6.4ns	7.6ns	22.4ns	22.6ns	
DVWH	15	Data Set-up to End of Write	15ns		5.8ns	6.6ns	6.2ns	6.8ns	6.6ns	7.4ns	6.8ns	7.6ns	7.2ns	8.0ns	7.0ns	7.4ns	
WHDX	16	Data Hold after End of Write	0ns		-4.4ns	-3.4ns	-4.8ns	-3.6ns	-5.2ns	-4.0ns	-5.4ns	-4.2ns	-5.6ns	-4.4ns	3.4ns	3.6ns	
AVWH	17	Address Set-up to End of Write	30ns		4.6ns	5.2ns	5.2ns	5.8ns	5.8ns	6.6ns	6.0ns	6.8ns	6.4ns	6.8ns	23.2ns	23.2ns	
AVWL	18	Address Set-up to Start of Write	0ns		-2.4ns	-1.6ns	-2.6ns	-1.8ns	-2.8ns	-2.0ns	-3.0ns	-2.0ns	-3.0ns	-2.0ns	1.6ns	1.8ns	
WHAX	19	Address Hold after End of Write	0ns		-2.2ns	-1.6ns	-2.2ns	-1.6ns	-2.4ns	-1.6ns	-2.2ns	-1.6ns	-2.4ns	-1.8ns	1.6ns	1.6ns	
WLQZ	20	Write Enable to Output Disable		15ns		11.0ns		11.8ns		12.7ns		13.8ns		14.4ns	0.6ns	1.2ns	
WHQX	21	Output Active after End of Write	3ns		28.4ns	31.2ns	30.2ns	33.8ns	32.6ns	37.8ns	34.2ns	39.0ns	34.8ns	40.0ns	25.4ns	27.2ns	
<b>WRITE CYCLE #2 (E/ Controlled)</b>																	
AVAV	12	Write Cycle Time	45ns														
WLEH	13	Write Pulse Width	30ns		3.6ns	5.0ns	4.2ns	5.4ns	4.8ns	6.2ns	5.0ns	6.4ns	5.2ns	6.6ns	23.4ns	23.6ns	
ELEH	14	Chip Enable to End of Write	30ns		5.6ns	6.6ns	6.0ns	7.2ns	6.6ns	7.8ns	6.6ns	8.0ns	6.8ns	8.0ns	22.0ns	22.0ns	
DVEH	15	Data Set-up to End of Write	15ns		5.2ns	5.4ns	5.4ns	6.0ns	6.0ns	6.6ns	6.2ns	6.8ns	6.4ns	7.0ns	8.0ns	8.2ns	
EHDH	16	Data Hold after End of Write	0ns		-3.8ns	-3.0ns	-4.2ns	-3.2ns	-4.8ns	-3.6ns	-5.0ns	-3.8ns	-5.0ns	-3.8ns	3.0ns	3.2ns	
AVEH	17	Address Set-up to End of Write	30ns		4.2ns	4.6ns	4.6ns	5.2ns	5.2ns	6.0ns	5.6ns	6.2ns	5.8ns	6.4ns	23.6ns	23.8ns	
AVEH	18	Address Set-up to Start of Write	0ns		-2.8ns	-1.8ns	-2.8ns	-2.0ns	-3.2ns	-2.2ns	-3.2ns	-2.4ns	-3.4ns	-2.4ns	1.8ns	2.0ns	
EHAX	19	Address Hold after End of Write	0ns		-1.6ns	-1.2ns	-1.8ns	-1.2ns	-2.0ns	-1.2ns	-2.0ns	-1.2ns	-2.0ns	-1.4ns	1.2ns	1.2ns	
<b>IV PARAMETERS</b>																	
AVAV	26	CE Controlled Initiation Cycle Time (Soft Seq)	45ns														
AVAV	26	OE Controlled Initiation Cycle Time (Soft Seq)	45ns														
AVELN	27	Address Set-up to Start of Write (Soft Seq)	0ns		-5.4ns	-4.0ns	-5.8ns	-4.2ns	-6.0ns	-4.6ns	-6.2ns	-4.6ns	-6.4ns	-4.8ns	4.0ns	4.2ns	
AVGL	27	Address Set-up to Start of OE (Soft Seq)	0ns		-5.4ns	-4.0ns	-5.6ns	-4.2ns	-6.0ns	-4.6ns	-6.2ns	-4.6ns	-6.2ns	-4.6ns	4.0ns	4.2ns	
ELEHN	28	Chip Enable to End of Write (Soft Seq)	30ns		3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	3.0ns	3.2ns	26.8ns	26.8ns	
GLGH	28	Output Enable Pulse Width (Soft Seq)	30ns		2.4ns	3.0ns	2.4ns	3.0ns	2.4ns	3.0ns	2.4ns	3.0ns	2.6ns	3.0ns	27.0ns	27.0ns	
ELAX	29	Address Hold after CE low (Soft Seq)	0ns		7.2ns	7.8ns	7.4ns	8.2ns	7.8ns	8.6ns	8.0ns	9.0ns	8.4ns	9.2ns	7.2ns	7.4ns	
GLAX	29	Address Hold after OE low (Soft Seq)	0ns		7.0ns	7.8ns	7.4ns	8.0ns	7.8ns	8.6ns	8.2ns	9.0ns	8.4ns	9.2ns	7.0ns	7.4ns	
ELQXS	23	Store Cycle Duration (Soft Seq)		15ms	11.4ms	13.3ms	9.9ms	11.1ms	8.3ms	9.6ms	8.1ms	8.7ms	7.7ms	8.3ms	1.7ms	3.9ms	
ELQXR	30	Recall Cycle Duration (Soft Seq)		50us	34.7us	40.5us	30.1us	33.6us	25.1us	29.0us	24.4us	26.4us	23.2us	25.2us	9.5us	16.4us	
VCCRIS	25	VCC Rise Time	150us														
DELAY	31	Time to Complete SRAM Cycle	1us														
HLHH	32	Hardware Store Pulse Width	15ns		3.8ns	5.0ns	3.8ns	5.2ns	4.0ns	5.6ns	4.2ns	5.8ns	4.2ns	6.0ns	9.0ns	9.2ns	
HLBL	33	Hardware Store Low to Store Busy		300ns													
<b>DC CHARACTERISTICS</b>																	
ICC1		Average Vcc Current @ AVAV=45ns		55mA	30.2mA	40.6mA	30.3mA	39.1mA	30.4mA	37.6mA	30.3mA	37.4mA	30.3mA	36.9mA	14.4mA	15.9mA	
ICC2		Average Vcc Current During Store		3mA	1.1mA	2.3mA	1.2mA	1.6mA	1.6mA	1.9mA	1.8mA	2.2mA	2.0mA	2.5mA	0.5mA	0.8mA	
ICC3		Average Vcc Current @200ns		10mA	7.0mA	7.6mA	7.3mA	8.2mA	7.7mA	8.2mA	7.7mA	8.3mA	7.9mA	8.6mA	1.4mA	1.7mA	
ICC4		Average Vcap Current during Autostore		3mA													
ISB		Vcc Standby Current		3mA	1.1mA	1.6mA	1.2mA	1.9mA	1.4mA	2.0mA	1.4mA	2.0mA	1.5mA	2.1mA	0.9mA	1.0mA	
ILKG		Input Leakage Current	-1uA	1uA													
IOLKG		Off-State Output Leakage Current	-1uA	1uA													
VIH		Input Logic "1" Level	2.2V		1.4V	1.9V	1.4V	1.9V	1.3V	1.9V	1.1V	1.9V	1.1V	1.9V	0.3V	0.3V	
VIL		Input Logic "0" Level		0.8V	1.1V	1.4V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	1.0V	1.4V	0.2V	0.2V	
VOH		Output Logic "1" Voltage	2.4V		2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	2.6V	3.5V	0.2V	0.2V	
VOL		Output Logic "0" Voltage		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VOLBU		Logic "0" Voltage on HSB1 Output		0.4V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.1V	0.3V	0.3V	
VSWITCH	24	Autostore Trigger Point		2.65V		2.48V		2.52V		2.57V		2.57V		2.57V			