Introduction

This document provides reliability data from qualifications and product monitors carried out on Simtek nvSRAM product.

Simtek product samples are tested to industry standard life test methods prior to release to production [product qualification] and at quarterly intervals during their production lifetimes. Details of test methods, sample size, and frequency are given in the following pages.

Product Families

Data is reported for product families using the same die and the same process technology. These are:
1] 4K, 16K and 64K products using 0.8 micron technology
2] 256K products using 0.8 micron technology
3] 256K and 1M products using 0.25 micron technology.

Major Manufacturing Sources

Simtek product is manufactured at subcontracted facilities. The major facilities are:
Foundry: Chartered Semiconductor Manufacturing, Fab 2, Singapore - 0.8 micron technology products
Foundry: Anam-DongBu Fab AFB1, S Korea - 0.25 micron technology products
Assembly: ASE, Chung-Li - 28 330 SOIC packages
Assembly: Amkor Technologies, ATP2, Philippines - all other package types
Package Level Test: Integra-Tech Services, Wichita, KS, USA - all packaged products
Package Level Test: Amkor Technologies, ATP3, Philippines - all packaged products
Package Level Test: Simtek Corporation, Colorado Springs, CO, USA. - ceramic packaged products

Additional Quality System, Package and Materials Data

Additional information including the ISO Quality Management Program, RMA and FA procedures, RoHS information, package thermal characteristics is available on Simtek's website at www.simtek.com

Contact

For more information contact Simtek at appseng@simtek.com

Product List

Simtek nvSRAM Products -Commercial & Industrial Temperature Range

Voltage	Density	Org	Part Number [STK-]	Die Source	Process Technology	Pins	SSOP	SOIC	PDIP	Package ID	25NS	35NS	45NS	Comments
3.0 V	1Mb	128Kx8	14CA8	1M	0.25 SONOS	32, 48	300	300		NF, RF	X	X	X	
3.0 V	256Kb	32Kx8	14D88	256K	0.25 SONOS	32, 48	300	300		NF, RF	X	X	X	
3.3 V	256Kb	32Kx8	16C88-3	256K	0.8 SNOS	32			600	WF		X		600 mil PDIP Package, Integrated Capacitor
3.3 V	256Kb	32Kx8	14C88-3	256K	0.8 SNOS	32		300		NF		X	X	
5.0 V	256Kb	32Kx8	16C88	256K	0.8 SNOS	32			600	WF		X		600 mil PDIP Package, Integrated Capacitor
5.0 V	256Kb	32Kx8	14C88	256K	0.8 SNOS	32		300		NF	X	X	X	AutoStore With Ext. Cap
5.0 V	256Kb	32Kx8	15C88	256K	0.8 SNOS	28		300 330		NF, SF	X		X	SRAM Compatible, AutoStore Without Ext. Cap
5.0 V	256Kb	32Kx8	11C88	256K	0.8 SNOS	28		300 330		NF, SF	X		X	SRAM Compatible, Software Store
5.0 V	64Kb	8Kx8	12C68	64K	0.8 SNOS	28		330	300 600	SF, WF, PF	X		X	SOIC, 600 mil PDIP, 300 mil PDIP
5.0 V	64Kb	8Kx8	11C68	64K	0.8 SNOS	28		330		SF	X	X	X	SOIC, Software Store
5.0 V	16Kb	2Kx8	22C48	64K	0.8 SNOS	28		300 330		NF, SF	X		X	SRAM Compatible

Simtek nvTime Products - Commercial & Industrial Temperature Range

Voltage	Density	Org	Part Number [STK-]	Die Source	Process Technology	Pins	SSOP	-	-	Package ID	25NS	35NS	45NS	Comments
3.0 V	1Mb	128Kx8	17TA8	1M	0.25 SONOS	32, 48	300			RF	X		X	With RTC, Watchdog Timer, Alarm, Power Reset
3.0 V	256Kb	32Kx8	17T88	256K	0.25 SONOS	32, 48	300			RF	X		X	With RTC, Watchdog Timer, Alarm, Power Reset

Simtek nvSRAM Products - Military & Extended Temperature Range

Voltage	Density	Org	Part Number [STK-]	Die Source	Process Technology	Pins	SB	LCC	-	Package ID	35NS	45NS	55NS	Comments
5.0 V	256Kb	32Kx8	14C88-5	256K	0.8 SNOS	32	300	450		L, C, K	X	X		gold or hot solder dip lead finish
5.0 V	64Kb	8Kx8	12C68-5	64K	0.8 SNOS	28	300	350		L, C, K	X		X	gold or hot solder dip lead finish
5.0 V	64Kb	8Kx8	11C68-5	64K	0.8 SNOS	28	300	350		L, C, K	X	X	X	gold or hot solder dip lead finish
5.0 V	64Kb	8Kx8	5962-94599	64K	0.8 SNOS	28	300	350		MX, MY	X		X	DESC Drawing, AutoStore
5.0 V	64Kb	8Kx8	5692-92324	64K	0.8 SNOS	28	300	350		MX, MY	X	X	X	DESC Drawing, Software Store

[package body width in mil]

Definitions

Sample Qtr

Production quarter represented by sample. Samples of production of major product lines are pulled quarterly for reliability testing.

Start / Rej

Number of devices started in the test.
Number of verified rejects from the test

Failure Rate

FIT rate = number of failures in 1E09 device hours. In accelerated tests where the acceleration factor is known, results are rated at 55C. Other failure rates are measured against the standard duration of the test method [eg failures per 1,000 cycles, 1,000 hrs]. All failure rates converted to 60% confidence.

Failure Anlaysis

Where there is a verified failure, details of the failure mode and failure mechanism are given. If FA is still open, this will be noted. if a specific corrective action was taken, this will be noted.

Sample Selection

Samples of each major production line are selected quarterly. All samples are taken from finished goods product. This means samples are typical of product shipped within the limits of the sample plan and sample frequency

HTOL Test

Same sample for both 168 [short term life/early life failure rate] and 1000hr + tests. Standard 168hr read point covers short term failures.

Endurance Test

Each nv cell in the array is subjected to repetitive store cycles with alternating data states. Devices are tested every 100k cycles to verify they are still functional. A failure is defined as one or more cells in the array failing to store or recall correct data. For all autostore parts, store cycles are initiated using both autostore and store.

Retention Test

Each nv cell in the array is stored with a 1 or 0 in a checkerboard pattern. Devices are then subjected to unbiased bake. The entire nv array is read at the read points. A failure is defined as a device with one or more cells failing to recall the original data state.

Reliability Test Methods

Qualification & Reliability Monitor Testing is based on JESD47 and JEDEC & Mil-Std-883 Test Methods

Test	Test Method	ID	Conditions	Duration	Units	SS	C	Monitor	Notes
DIE RELATED									
Functional & Data Sheet Parameters	Simtek Data Sheet	Electrical Test Program	Ind temp range		-	77	0	Each Qtr Device Type	Datasheet Characterization
Data Retention	Jedec 22 Simtek	A103	150C Unbiased	1,000	Hrs	77	0	Qtr Die Type	Qual & Major Change
Endurance	Simtek	Store/Recall Cycles	25C Datasheet	to spec	Cycles	64	0	Qtr Die Type	Qual & Major Change
HTOL	Mil-Std-883	M1005	Vcc Nom 125C	1,000	Hrs	77	1	Qtr Die Type	Qual & Major Change
ESD Classification	Jedec	A114	HBM & CDM			9	0		Qual & Major Change
Latch-Up Integrity	Jedec	78	±150mA, 70C [min]			6	0		Qual & Major Change
I/O Capacitance	Mil-Std-883	M3012	Data Sheet			5	0		Qual & Major Change
PACKAGE RELATED									
Dimensions, External Visual	Simtek Data Sheet	B100	Pkg Outline Dimensions		-	15	0	Annual Pkg Type	Qual & Pkg Change
Resistance To Solvents	Jedec 22	B107	3 Solvents		-	15	0	Annual Pkg Type	Qual & Pkg Change
Solderability	Jedec 22	B102	IR Reflow Solder Bath		-	22	0	Annual Pkg Type	Qual & Pkg Change
Temp Cycle	Jedec 22	A104	-40C To +125C	1,000	Cycles	45	0	Annual Pkg Type	Qual & Pkg Change
Temp Humidity Bias	Jedec 22	A101	85/85 Vcc Nom	1,000	Hrs			Annual Pkg Type	Qual & Pkg Change
PCT [Autoclave]	Jedec 22	A102	121C/2Atm/ 100% RH	168	Hrs	45	0	Annual Pkg Type	Qual & Pkg Change
Pkg Preconditioning	Jedec 22	A113C	Per Pkg MSL		-	N/A	N/A		Per JESD47 TC & PCT
Moisture Sensitivity	J-Std-020	To Max Passing Level, For Plating Type				22	0		Qual & Pkg Change

Activation Energies

Activation Energy Associated With Failure Mechanisms [Arrhenius]

Failure Mechanism	Activation Energy
Ionic Contamination	1.0Ev
Gate Oxide/ Dielectric Breakdown	0.3Ev - 0.6Ev
Electromigration	0.5Ev
Slow Trapping	1.3Ev
Corrosion	0.7Ev
Intermetallic Formation	0.8Ev
Bond Failure [Al/Au]	1.0Ev
Packaging Corrosion	0.7Ev
Unknown	0.7Ev

Retention Acceleration For SNOS and SONOS Non-Volatile Cells

The charge held in the nitride layer of an SNOS & SONOS cell decays over time. The nvsram cell design allows the charge to be measured via the cell vt. The vt decay of non-volatile cells for a given snos manufacturing process can therefore be characterized over time and temperature, as well as for process corners. In addition, it is possible to review the distribution of decay rates across all cells in the array and to identify the fastest decaying cells in the array. This also allows for effective retention screening of individual die at wafer level by eliminating die which contain cells with decay rates which would result in retention times of less than 100 years at 55C. Infant mortality due to cell defects is therefore eliminated.

The predominant latent failure mechanism for SNOS/SONOS retention is charge decay [vt decay] over time. The failure occurs when the vt drops to a level that prevents the state of the cell from being read. To establish the relationship between bake temperature and vt, a large number of entire wafers were baked over extended periods at temperatures ranging from 25C through 250C. The vt of the worst case cells [worst performing bit] in each die were measured at multiple readpoints, and the results plotted against log time in seconds.

The resulting plots show vt decay to be linear against log time in decade seconds under temperature accelerated conditions [t1 = (t2)(acceleration factor)] [1]. In the standard Arrhenius model, af is defined as the ratio of times to failure, or the ratio of the test time at higher temperature to the equivalent time at operating temperature. The time acceleration due to temperature for a given ea, af and t1 and t2 is linear (t1 = t2 x acceleration factor).

This result means that the retention failure mechanism for SNOS is highly accelerated by temperature. It is therefore possible to simulate a very long time at operating temperature using relatively short accelerated test times at reasonable test temperatures for plastic encapsulated devices. the reliability data collected from Simtek nvSRAM devices shows exceptional retention reliability. These results have been validated by very low retention failure rates reported in the field. [see field reliability return analysis sheet].

The following example demonstrates the difference between a typical oxide breakdown type of failure mechanism and vt decay in an SNOS/SONOS cell.

Arrhenius Equation: **Af = (E) [(Ea/K)(1/T1-1/T2)]**

For An Unbiased Retention Test At 150C For 1000 Hours, Comparing A Predominant Failure Mechanism Of Charge Loss Through Dielectric Breakdown Against SNOS Vt Decay.

	Ea	0.6	Activation Energy For Charge Loss.
	Edr	0.0593	Based On Charn Of Vt Decay Rate
	K	0.00008625	
	Deg C	Deg K	
T1	55	328	
T2	150	423	
	Hrs	Years	
T2	1,000	0.11	
Arrhenius Solution For Af, Ea = 0.6	**Af =**	**117.12**	

Applying Af [Ratio Of Times To Failure] For T1=(T2)X(Af) For A Charge Loss Failure Mechanism:

	Hrs	Years
T1 =	117,124	13.37
Arrhenius Solution For Af, Edr = 0.059	**Af =**	**1.60**

Applying Af [Ratio Of Decay Rates] For T1=(T2)Af For The SNOS Failure Mechanism:

	Hrs	Years
T1 =	8,745,420	998.34

[1]: SNOS-Based nvSRAM Data Retention. P Ruths Et Al. NV Semiconductor Memory Workshop, Monterey, CA 1997.

Example Failure Rate Calculations

Example Failure Rate Calculation For HTOL

100 Devices, 2,000Hr @ 140C, 1 Gox Failure., 60% Confidence @ 55C:

Total Devices	1,116	
Average Hrs/Test	1,000	
Test Temp	125	
Total Device Hrs	1,116,000	@140C
# Failures	0	
Failure Mechanism[S]		Probable Gate Oxide Breakdown
Acceleration Factor For 125C Vs 55C @ 0.7Ev	77.82	0 Fails, "Unkown" Mechanism.
Half Chi2 Factor For 0 Fails, 60% Cl	0.917	
Acceleration Factor For 125C Vs 55C @ 0.3Ev	77.82	1 Fail, Oxide Breakdown
Half Chi2 Factor For 1 Fails, 60% Cl	0.000	
Estimated Failure Rate [Fits] @ 55C, 60% Ucl	**10.6**	Fits. Oxide Breakdown Has A Low Activation Energy Which Contributes Heavily To The High Calculated Failure Rate.

Example Failure Rate Calculation For Endurance

250 Devices, 1M Cycles Each, 1 Failure @ 60% Confidence:

Total Devices	250	
Cycles Per Device	1M	
Test Temp	25C	
Total Device Cycles	250,000,000	
# Failures	1	
Failure Mechanism[s]		Pump
Acceleration Factor	1.00	
Half Chi2 Factor For 1 Fail, 60% Cl	2.023	
Estimated Failure Rate Per 1M Cycles 60% Ucl	**0.81**	%

Example Failure Rate Calculation For Retention

1500 Devices, 1,000Hr @ 150C, 1 Recall Failure, 60% Confidence @ 55C:

Total Devices	350	
Average Hrs/Test	1,000	
Test Temp	150C	
Total Device Hrs	350,000	@150C
# Failures	1	
Failure Mechanism[s]		Leakage From SNOS Cell [Accelerated Vt Decav Rate]
Af For Edr 0.05963	1.6	
Acceleration Factor For 150C Vs 55C	1,450	Per SNOS Decay Rate Characterization
Half Chi2 Factor For 0 Fails, 60% Cl	0.917	For "Zero" Fails
Af For Edr 0.0593	1.6	Per SNOS Decay Rate Characterization.
Half Chi2 Factor For 1 Fail, 60% Cl	2.023	
Estimated Failure Rate [Fits] @ 55C, 60% Ucl	**0.4**	Fits. Temperature Acceleration For Charge Decay In The Memory Nitride Layer Is High, And Contributes To The Very Low Failure Rate At 55C. See Activation Energy Summary On Previous Pages.

High Temperature Operating Life Summary Data

HTOL [note 1]	JEDEC 22	A108	Dynamic, 125C, Vcc max [note 2]	FIT rate @ 55C, 60% ucl

Early Life Failure Rate [@ 168hrs 125C]						
technology	part family	sample size	rejects	PPM	FITs	Failure Information / Corrective Action
0.8	**4K, 16K & 64K**	**1,241**	**0**	**0**	**19**	
0.8	**256K 5V**	**2,373**	**0**	**0**	**17**	
0.8	**256K 3V**	**2,343**	**1**	**427**	**29**	04Q3 AC fail. Increased temp gdbanding.
0.25	**256K 3V**	**731**	**0**	**0**	**96**	Small sample size
0.25	**1M 3V**	**1,823**	**0**	**0**	**38**	

1,000 Hr/125C FAILURE RATE						
technology	part family	sample size	rejects	PPM	FITs	Failure Information / Corrective Action
0.8	**4K, 16K & 64K**	**1,241**	**0**	**n/a**	**3**	
0.8	**256K 5V**	**2,373**	**0**	**n/a**	**3**	
0.8	**256K 3V**	**2,343**	**1**	**n/a**	**17**	
0.25	**256K 3V**	**731**	**0**	**n/a**	**20**	
0.25	**1M 3V**	**1,823**	**2**	**n/a**	**21**	05Q2 Col fail 1Khr. Fab process change.

Note 1: Key timing parameter variation after HTOL lifetest is also evaluated.

Note 2: 0.25 technology devices with on-board voltage regulation are tested with an external Vcc of 3.6V and an internally regulated Vcc of 2.4V.

NV Store Cycle Endurance Summary Data

Store to, Recall from NV Array [note 1]	Simtek	25C [note 2]	Store 1, Store 0 in all nv array locations. 10x store/recall verification cycles every 50K Store cycles. Note: Read/Write to SRAM unlimited. Endurance is measure of reliability of Store/Recall to and from NV array from SRAM array.

NV Store/Recall Failure Rate @ Specification Limit						
technology	part family	Spec	sample size	rejects	PPM	Failure Information/Action
0.8	**4K, 16K & 64K**	**1M**	**2,817**	**1**	**355**	Single bit failure to recall correct data
0.8	**256K 5V**	**1M**	**2,613**	**1**	**383**	Single bit failure to recall correct data
0.8	**256K 3V**	**1M**	**2,042**	**2**	**979**	Single bit failure to recall correct data
0.25	**256K 3V**	**200K**	**1,575**	**0**	**0**	
0.25	**1M 3V**	**200K**	**3,552**	**2**	**563**	06Q2: Adjust trim to add margin.

Note 1: Testing for Store/Recall reliability is carried out using both Autostore/Power Cycle and softstore modes.

Note 2: Design and technology characterization testing is also carried out at min and max temp.

NV Retention Summary Data

NV Array Retention	Unbiased Bake @ 150C. Store Checker Board Pattern To Nv Array. Failure Rate @ Operating Temp In Fits @ 60%Ucl.						
Non-Volatile Retention @ Specification Limit							
Technology	Part Family	Spec	Sample Size	55C	70C	85C	Failure Information / Corrective Action
0.8	**16K & 64K**	**100yr**	**2,417**	**0**	**5**	**116[*]**	Stored Data Recall failures
0.8	**256K 5V**	**100yr**	**1,710**	**0**	**7**	**280[*]**	Stored Data Recall failures
0.8	**256K 3V**	**100yr**	**2,024**	**0**	**0**	**142[*]**	Stored Data Recall failures
0.25	**256K 3V**	**20yr**	**1,438**	**8**	**16**	**425[*]**	Stored Data Recall failures
0.25	**1M 3V**	**20yr**	**2,054**	**0**	**3**	**146[*]**	Stored Data Recall failures

*Data From End Of Life Studies.

EOL: Beyond Std sample 1Khr/150C Test Duration. End Of Life Data In Preparation.

ESD & Latch-Up

PRODUCT ESD CLASSIFICATION

MIL-STD-883	M3015/J22-A114	Human Body Model
JEDEC 22	J22-C101	Charged Device Model

Part Number	Passing Level [HBM]	Passing Level [CDM]
STK20C04	1850V	500V
STK10C48	1850V	500V
STK11C48	1850V	500V
STK22C48	1850V	500V
STK25C48	1850V	500V
STK10C68	1850V	500V
STK11C68	1850V	500V
STK12C68	1850V	500V
STK15C68	1850V	500V
STK16C68	1850V	500V
STK11C88	1850V	500V
STK14C88	1850V	500V
STK15C88	1850V	500V
STK16C88	1850V	500V
STK11C88-3	>2000V	500V
STK14C88-3	>2000V	500V
STK16C88-3	>2000V	500V
STK14D88	>2000V	500V
STK17T88	1500V	500V
STK14CA8	>2000V	500V
STK17TA8	1500V	500V

LATCH-UP

JESD97	IC Latchup Test

All products are rated at ±150mA at 70C minimum.