



Simtek Corporation

4250 Buckingham Drive, Suite 100
Colorado Springs, CO 80907 USA
Tel: 719-531-9444 Fax: 719-531-948

PRODUCT QUALIFICATION REPORT

Fab Line Change: 256K 5V nvSRAM

STK14C88 [military temperature]

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SUMMARY

The wafer foundry line for Simtek 256K nvSRAM Military Temperature Range products has changed from Fab 1 to Fab 2 at Chartered Semiconductor Manufacturing in Singapore. The revision level of the product has changed from Rev C (Fab 1) to Rev D (Fab 2). There are significant changes in the design or the manufacturing process.

The new products completed commercial qualification in mid-2004. Military temperature range devices for this product line are built on EPI substrate to improve Latch-Up performance at high temperature. All other design and process characteristics are identical to the commercial product line.

There are no changes to any electrical or mechanical data sheet specifications. To ensure consistency of product characteristics, Simtek has completed a comparison of the electrical performance between devices manufactured in Fab 1 and Fab 2. This report details the results of this comparison and confirms the consistent characteristics of product built on both Fab lines.

PRODUCT AFFECTED

STK14C88-LE

STK14C88-LM [non-compliant Mil-Std-883]

STK14C88-CE

STK14C88-CM [non-compliant Mil-Std-883]

NEW PRODUCT DESIGN REV ID

Products out of Fab 2 will be marked "**Simtek D**" on the first line of the topside mark. The previous revision ID was "Simtek C".

CHANGE DETAIL

- This line move is from Chartered Semiconductor's Fab 1 [CSM1] to Fab 2 [CSM2].
- The Simtek nvSRAM design has been transferred to the new line without change.
- The product is being built to the same 0.8 micron design as in CSM1.
- The CSM2 product meets the current datasheet specifications as published on the Simtek website www.Simtek.com.
- No changes have been made in assembly or final test & burn-in.

PCN RREFERENCE

PCN 10028 Rev 00 issued October 04 2005.



Process Characterization Report

Comparison of CSM1 and CSM2 key process parameters affecting device functionality.

Parameter	Unit	% Change	Comments
NLLS Vtlin	Volt	6%	
NLLS Idsat	mA	-3%	
NLLS Bvdss	Volt	3%	
PLLS Vtlin	Volt	4%	
PLLS Idsat	mA	-5%	
PLLS Bvdss	Volt	2%	
NHLS Vtlin	Volt	10%	
NHLS Idsat	mA	-5%	
NHLS Bvdss	Volt	8%	
PHLS Idsat	mA	-3%	
PHLS Bvdss	Volt	4%	
SNOS Icell Ik	uA	0%	
VMG Positive Vstop	Volt	1%	
VMG Negative Vstop	Volt	1%	
NLV Bkn	Volt	1%	
PLV Bkn	Volt	0%	
NHV Bkn	Volt	3%	
PHV Bkn	Volt	2%	
NLP1 Vtsat	Volt	-7%	
NHP 2 Vtsat	Volt	-6%	
Ndiff	Ohm/Sq	-4%	
Pdiff	Ohm/Sq	-5%	
Npoly1	Ohm/Sq	-3%	
NPoly2	Ohm/Sq	8%	
N Contact	Ohm	4%	
P Contact Ohm/con	Ohm	27%	* Due to use of different/better barrier metal material
M1/M2 Via	Ohm	-8%	
Buried Contact 1 Rcon	Ohm	4%	
Buried Contact 2 Rcon ohm/con	Ohm	2%	

Summary

Absolute wafer level e-parameter values are proprietary to Simtek and the Wafer Foundry.

All values for the CSM2 process correlate well with the original CSM1 process and remain well within the original CSM1 process specification limits.



Qualification Lifetest Report
 CSM2 0.8μ CMOS/SNOS Process, Simtek 256K 5V nvSRAM

Test	Method	Conditions	Readpoint	Start Qty	# of Failures	Failure Detail
High Temperature Operating Life [HTOL]	JESD-22 A108	Dynamic Full SRAM Array 125C Vcc nom 4 Fab Lots	0 hrs	467	0	zero fails @ 1K hrs.
			168 hrs	467	0	
			500 hrs	467	0	
			1000 hrs	467	0	
Retention	Simtek	Unbiased Bake 150C Store nv array at 0 hr Read stored data at read points 4 Fab Lots	0 hrs	400	0	1 fail at 10yr/70C equivalent ^[1] Corrective action: Adjust retention screen limit. 1 fail at 10yr/85C equivalent ^[1] Corrective action: Adjust retention screen limit. 2 fails through 1K hrs ^[1] Corrective actions complete & verified.
			48 hrs	400	0	
			168 hrs	400	1	
			500 hrs	399	1	
Endurance	Simtek	Store/Recall cycles of nv array Recall and Functional check at read points	0 cycles	269	0	Zero fails @ 1M cycles.
			100K cycles	269	0	
			500K cycles	269	0	
			1M cycles	269	0	
ESD	JEDSD22 A114	Human Body Model		5	0	Pass 1.8KV
Latch-Up Integrity	JEDEC 78	± 200mA, 85C		6	0	Pass ±200mA, 85C

Note 1: 2 failures recorded in retention testing [store NV array followed by unbiased bake with interim readpoints to verify stored data pattern is no corrupted and all cells read correct data state]. Wafer level retention screening limits adjusted to provide greater margin against Data Sheet Retention specification.



STK14C88 Characterization: Comparison between Revision C and Revision D

SYMBOL	#	PARAMETER	-45 SPEC		Mil MTS [°]	Fab 2			Fab 1			Fab1 Fab2 Diff	Worst Case Condition
						mean	stdev	Cpk	mean	stdev	Cpk		
READ CYCLE 1 & 2			MIN	MAX									
ELQV	1	Chip Enable Access Time		45ns	21.2	23.8	0.5	14.13	23.8	0.4	17.67	0.00	125C / 4.5V
AVAV	2	Read Cycle Time	45ns		22.7	22.3	0.5	15.13	22.2	0.3	25.33	0.10	125C / 4.5V
AVQV	3	Address Access Time		45ns	19.6	25.4	0.5	13.07	24.8	0.4	16.83	0.60	125C / 4.5V
GLQV	4	Output Enable to Data Valid		20ns	14.3	5.7	0.3	15.89	4.9	0.5	10.07	0.80	125C / 4.5V
AXQX	5	Output Hold after Address Change	5ns		7.3	12.3	0.6	4.06	11.7	0.4	5.58	0.60	-55C / 5.5V
ELQX	6	Chip Enable to Output Active	5ns		7.4	12.4	0.3	8.22	12.1	0.3	7.89	0.30	-55C / 5.5V
EHQZ	7	Chip Disable to Output Inactive		15ns	9.7	5.3	0.3	10.78	5.2	0.3	10.89	0.10	125C / 4.5V
GLQX	8	Output Enable to Output Active	0ns		4	4	0.2	6.67	3.2	0.4	2.67	0.80	-55C / 5.5V
GHQZ	9	Output Enable to Output Inactive		15ns	9.7	5.3	0.6	5.39	4.9	0.5	6.73	0.40	125C / 4.5V
ELICCH	10	Chip Enable to Power Active	0ns			N/A	N/A	N/A	N/A	N/A	N/A		Note F
EHICCL	11	Chip Disable to Power Standby		45ns		N/A	N/A	N/A	N/A	N/A	N/A		Note F
WHQV	12	Write Recovery Time		45ns	18.8	26.2	0.6	10.44	26.2	0.5	12.53	0.00	125C / 4.5V
WRITE CYCLE #1			MIN	MAX									
AVAV	13	Write Cycle Time	45ns		22.7	22.3	0.5	15.13	22.2	0.3	25.33	0.10	125C / 4.5V
WLWH	14	Write Pulse Width	30ns		16.2	13.8	0.6	9.00	14	0.5	10.67	-0.20	125C / 4.5V
ELWH	15	Chip Enable to End of Write	30ns		17.8	12.2	0.4	14.83	12.5	0.4	14.58	-0.30	125C / 4.5V
DVWH	16	Data Set-up to End of Write	15ns		8.1	6.9	0.5	5.40	6.9	0.5	5.40	0.00	125C / 4.5V
WHDX	17	Data Hold after End of Write	0ns		2.2	-2.2	0.4	1.83	-2.2	0.3	2.44	0.00	125C / 4.5V
AVWH	18	Address Set-up to End of Write	30ns		25	5.0	0.4	20.83	4.6	0.5	16.93	0.40	125C / 4.5V
AVWL	19	Address Set-up to Start of Write	0ns		3.2	-3.2	0.3	3.56	-3.3	0.3	3.67	0.10	-55C / 5.5V
WHAX	20	Address Hold after End of Write	0ns		1.8	-1.8	0.3	2.00	-1.9	0.2	3.17	0.10	-55C / 5.5V
WLQZ	21	Write Enable to Output Disable		15ns	7.6	7.4	0.3	8.44	7.2	0.3	8.67	0.20	125C / 4.5V
WHQX	22	Output Active after End of Write	5ns		8.4	13.4	0.4	7.00	13.2	0.4	10.67	0.20	-55C / 5.5V
WRITE CYCLE #2			MIN	MAX									
AVAV	23	Write Cycle Time	45ns		22.7	22.3	0.5	15.13	22.2	0.3	25.33	0.10	125C / 4.5V
WLEH	24	Write Pulse Width	30ns		16.4	13.6	0.4	13.67	13.7	0.3	18.11	-0.10	125C / 4.5V
ELEH	25	Chip Enable to End of Write	30ns		23.8	6.2	0.2	39.67	6.5	0.2	39.17	-0.30	125C / 4.5V
DVEH	26	Data Set-up to End of Write	15ns		8	7	0.4	6.67	7	0.3	8.89	0.00	125C / 4.5V
EHDX	27	Data Hold after End of Write	0ns		2.2	-2.2	0.4	1.83	-2.2	0.3	2.44	0.00	-55C / 5.5V
AVEH	28	Address Set-up to End of Write	30ns		19.3	10.7	0.6	10.72	9.7	0.4	16.92	1.00	125C / 4.5V
AVEL	29	Address Set-up to Start of Write	0ns		2.3	-2.3	0.4	1.92	-2.5	0.3	2.78	0.20	-55C / 5.5V
EHAX	30	Address Hold after End of Write	0ns		1.9	-1.9	0.4	1.58	-2.1	0.3	2.33	0.20	-55C / 5.5V



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SYMBOL	#	PARAMETER	-45 SPEC		Mil MTS [°]	Fab 2			Fab 1			Worst Case Condition	
						mean	stdev	Cpk	mean	stdev	Cpk		
			MIN	MAX	Fab 2		Fab 1		Fab1 Fab2				
HARDWARE STORE CYCLE			MIN	MAX									
tSTORE	31	Store Cycle Duration (HLHZ)		10mS	3.3	6.7	0.5	2.20	6.8	0.5	2.13	-0.10	125C / 4.5V
tDELAY	32	time allowed to complete SRAM cycle (HLQZ)	1us		0.28	1.28	0.05	1.87	1.33	0.05	2.20	-0.05	125C / 4.5V
HHQX	33	Hardware store high to inhibit off		700ns	75	625	15	1.67	665	11	1.06	-40.00	125C / 4.5V
HLHX	34	Hardware store pulse width	15ns		10.6	4.4	0.3	11.78	4.4	0.3	11.78	0.00	125C / 4.5V
HLBL	35	Hardware store low to store busy		300ns	187	113	15	4.16	120	16	3.75	-7.00	125C / 4.5V
AUTOSTORE / POWERUP RECALL			MIN	MAX									
tRESTORE	36	Power Up Recall Duration		550us	185	365	20	3.08	410	25	1.87	-45.00	125C / 4.5V
tSTORE	37	Store Cycle Duration (HLHZ)		10ms	3.3	6.7	0.5	2.20	6.8	0.5	2.13	-0.10	125C / 4.5V
tVSBL	38	Vswitch to HSB low		300ns	187	113	15	4.16	120	16	3.75	-7.00	125C / 4.5V
tDELAY	39	Time Allowed to Complete SRAM cycle (BLQZ)	1us		1	1.2	0.01	6.67	1.2	0.01	6.67	0.00	125C / 4.5V
Vswitch	40	Low voltage trigger level	4.0V	4.5V	0.17	4.17	0.04	1.42	4.08	0.03	0.89	0.09	125C / 4.5V
Vreset	41	Low voltage Reset level		3.6V	0.5	3.1	0.1	1.67	3.05	0.05	3.67	0.05	125C / 4.5V
SOFTSTORE / RECALL CYCLE			MIN	MAX									
AVAV	42	Store/Recall Initiation Cycle	45ns		22.7	22.3	0.5	15.13	22.2	0.3	25.33	0.10	125C / 4.5V
AVEL	43	Address Setup Time	0ns		2.3	-2.3	0.4	1.92	-2.5	0.3	2.78	0.20	-55C / 5.5V
ELEH	44	Clock Pulse Width	30ns		23.8	6.2	0.2	39.67	6.5	0.2	39.17	-0.30	125C / 4.5V
ELAX	45	Write Enable Setup	20ns		7.1	12.9	0.3	7.89	13	0.3	7.78	-0.10	125C / 4.5V
tRECALL	46	Nonvolatile Enable fall to Outputs inactive		20us	6.6	13.4	0.6	3.67	13.8	0.5	4.13	-0.40	125C / 4.5V
DC CHARACTERISTICS			MIN	MAX									
ICC1	47	Average Vcc Current @ AVAV=45ns		70mA	19	51	1	6.33	54	1.5	3.56	-3.00	125C / 55V
ICC2	48	Average Vcc Current During Store		6mA	2.85	3.15	0.05	-1.00	3.1	0.1	-0.33	0.05	-55C / 5.5V
ICC3	49	Average Vcc Current @200ns, 5.0V, 25C		10mA	10								Note G
ICC4	50	Average Vcap current during Autostore		2mA	0.6	1.4	0.1	2.00	1.22	0.1	2.60	0.18	-55C / 5.5V
ISB1	51	Average Standby @ 45ns		23mA	1.5	21.5	0.6	0.83	19	0.4	3.33	2.50	-55C / 5.5V
ISB2	52	Icc Standby Current (Static CMOS Levels)		3mA	1.0	2	0.02	-8.33	1.85	0.01	-11.67	0.15	-55C / 5.5V
ILKG	53	Input Leakage Current	-1uA	1uA	N/A	N/A	N/A	N/A	N/A	N/A	N/A		Note H
IOLKG	54	Off-State Output Leakage Current	-5uA	5uA	N/A	N/A	N/A	N/A	N/A	N/A	N/A		Note H
VIH	55	Input Logic "1" Level	2.2V		0.47	1.73	0.1	1.57	1.74	0.1	1.53	-0.01	-55C / 5.5V
VIL	56	Input Logic "0" Level		0.8V	0.19	0.99	0.04	1.58	1	0.05	1.33	-0.01	-55C / 5.5V
VOH	57	Output Logic "1" Voltage	2.4V		1.4	3.8	0.04	11.67	3.3	0.05	6.00	0.50	125C / 4.5V
VOL	58	Output Logic "0" Voltage		0.4V	0.14	0.26	0.03	1.56	0.25	0.04	1.25	0.01	125C / 4.5V
VBL	59	Logic "0" Voltage on HSB Output		0.4V	0.29	0.11	0.01	9.67	0.115	0.02	4.75	-0.01	23C

Note F Guaranteed not tested [verified by design].
 Note G Typical value. No specification. See datasheet.
 Note H Parameter not tested in characterization but screened in package level test.
 Mil MTS Military temperature margin to specification

Specification is the Simtek 1999 data book specification for the STK14C88-M, 45ns device. This specification will be published on the Simtek website in the near future.